

ECEN 474/704 Lab 1: Introduction to Cadence & MOS Device Characterization

Objectives

Learn how to login on a Linux workstation, perform basic Linux tasks, and use the Cadence design system to simulate circuits. Cadence will also be used to understand and measure transistor model parameters.

Introduction

This lab will introduce students to the computer system and software used throughout the lab course. First, students will learn how to login and logout of a Linux workstation. Next, basic operating system commands used to perform file management, printing, and various other tasks will be illustrated. Finally, students will be given an overview of the Cadence Development System.

In-class examples will demonstrate the creation of libraries, the construction of schematic symbols, the drafting of schematics, and the layout of simple transistors. The student will apply this knowledge to the creation of a CMOS inverter.

This lab will also review basic transistor operation and you will learn how the SPICE model parameters relate to the physical structure and electrical equations of the device. Then you will measure various electrical model parameters: V_{T0} , λ , KP and γ .

Logging-In/Logging-Out

In order to use the Linux machines, you must first login to the system. As with the PC lab, login using your TAMU NetID and password (same login ID and password used to log into the "HOWDY" portal). This is your ECE Linux account and all files stored in this area will be retained by the system after logging-out.

Using the Linux Operating System

Using the Linux operating system is similar to using other operating systems such as DOS. Linux commands are issued to the system by typing them into a "shell" or "xterm". Linux commands are case sensitive so be careful when issuing a command, usually they are given in lower-case.

The following list (Table 1-1) summarizes some basic commands required to manage the data files you will be creating in this lab course. All Linux commands are entered from the shell or xterm window. Do not use Linux commands for modifying, deleting, or moving any Cadence data files.

Table 1-1: Common UNIX Commands

ls -al	Lists all files in current directory, including hidden files
ll	Lists all files in current directory with time stamps and permissions
mkdir XXXX	Creates a new directory titled "XXXX"
cd XXXX	Changes the current directory to "XXXX"
cd ..	Changes the current directory back one level
cd ~	Changes the current directory back to the home directory
cp XXXX YYYY	Copies file "XXXX" to file "YYYY"
mv XXXX YYYY	Moves (or renames) file "XXXX" to file "YYYY"
rm XXXX	Deletes file "XXXX"

gedit XXXX &	Opens file "XXXX" using the text editor "gedit", "&" returns the prompt to the shell
clear	Clears the screen (alternatively, you can press Ctrl-L)
top	Shows the process/memory table (press q to exit)
\rm -rf XXXX	Removes the file or directory "XXXX" without any confirmation

Task Manager in Linux

If you type `ps -ef | grep <NetID>`, it will list the processes running on the system. If for some reason Cadence, Virtuoso or Calibre crashes or freezes, the process could still be running and slowing down the server without doing anything. Using the "ps" command above you can find the index number (in the first column of the list next to NetID) of the process. Now if you type `kill -9 <index number>`, you can kill the process. You can also issue the command `kill -1 -1` to kill all your processes.

Cadence

The Cadence Development System consists of a bundle of software packages such as schematic editors, simulators and layout editors. This software manages the development process for analog, digital and mixed-signal circuits. In this course, we will strictly use the tools associated with analog circuit design.

All the Cadence design tools are managed by a software package called the Design Framework II. This program supervises a common database which holds all circuit information including schematics, layouts, and simulation data. From the Design Framework II, also known as the "framework", we can invoke a program called the "Library Manager" which governs the storage of circuit data. We can access libraries and the components of the libraries called cells.

Also, from the framework we can invoke the schematic entry editor called "Composer". Composer is used to draw circuit diagrams and draw circuit symbols. A program called "Virtuoso Layout Suite" is used for creating integrated circuit layouts. The layout is used to create the masks which are used in the integrated circuit fabrication process.

Finally, circuit simulation is handled through an interface called Analog Design Environment (ADE). This interface can be used to invoke various simulators including HSPICE, Spectre, UltraSim, and Verilog. We will be using the Spectre simulator in this course.

Starting Cadence

After logging into a Linux workstation in the lab using your NetID and password, the first step is to open a Terminal using the menu item *Applications*→*Favorites*→*Terminal* (Figure 1-1), or using the right-click menu on the desktop. The next step is to create a new directory (Figure 1-2) that will keep all Cadence designs for the ECEN 474/704 lab. This directory can be used only for one technology (for this course, IBM 180nm). If you need to use another process for a different project or course, you need to create another directory.

Never start Cadence directly from your home directory, always change directory (cd) into the subdirectory corresponding to the technology you will use, then start Cadence as follows:

```
cd lab-ibm180
/disk/amsc/bin/ibm180
```

This will load Cadence. The Command Interpreter Window (CIW) will now load as shown in Figure 1-3. If you are outside the Linux lab room, you can connect to ECE servers using a secure shell (ssh) from another computer on campus or a personal computer. If the computer has Linux or Unix operating system, you can use the following commands to connect to ECE Linux servers:

```
ssh -X NetID@apollo.ece.tamu.edu
ssh -X NetID@hera.ece.tamu.edu
```

At the prompt, you need to type your password. If you are connecting from a computer that has a Windows or Apple operating system, you need to have an ssh client and an X-server installed (putty and xming are two examples, respectively). Make sure that X11 connections are tunneled within the settings of the ssh client you are using. Once you login, you can start Cadence using the same commands.

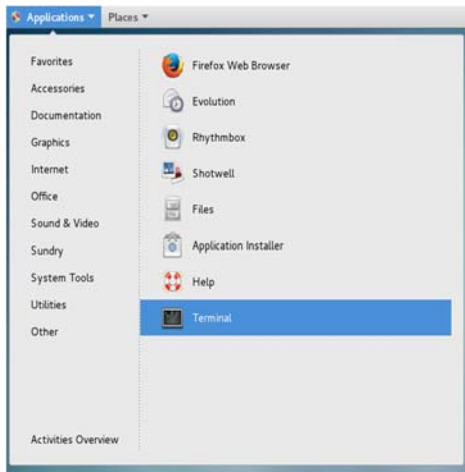


Figure 1-1: Accessing the Terminal

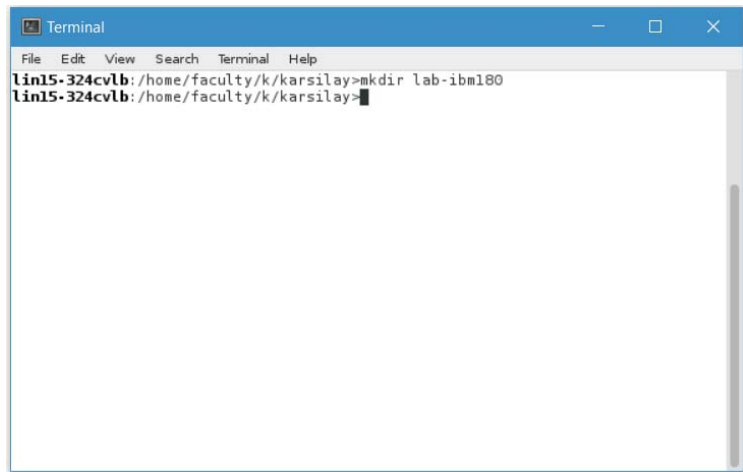


Figure 1-2: Creating a directory in the Terminal

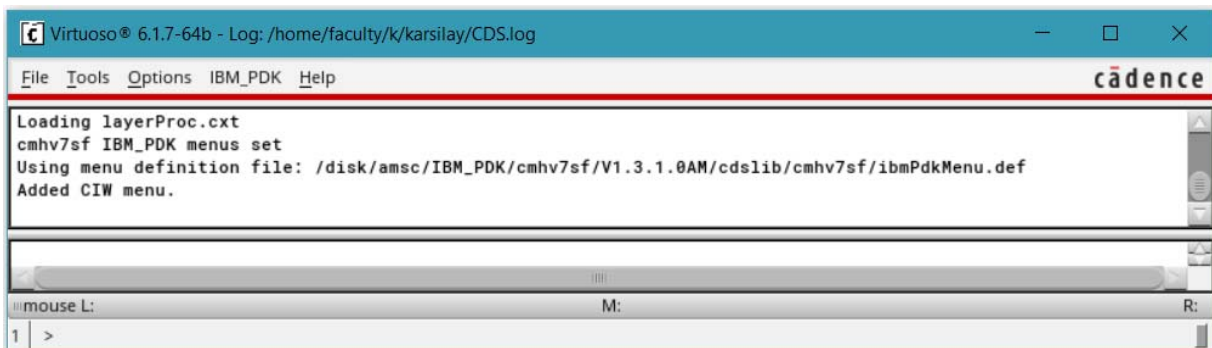


Figure 1-3: The Cadence Command Interpreter Window (CIW)

Creating a New Library

From the CIW (Figure 1-3) select *Tools*→*Library Manager* to load the library manager (Figure 1-4). The Library Manager stores all designs in a hierarchal manner. A library is a collection of cells. For example, if you had a digital circuits library named Digital, it will have several cells included in it. These cells will be inverters, nand gates, nor gates, multiplexers, etc. Each cell has different views. These views will be symbols, schematics, or layouts of each cell.

The first thing you need to do to start a design is create a library to store the cells you will be designing in this lab. Let's call this library "Lab1". From the Library Manager window select *File*→*New*→*Library*. Name the library "Lab1" (without the quotes) and select OK. In the popup window that appears select "Attach to an existing technology library" (Figure 1-5) and select OK. In the next window make sure the **cmhv7sf** Technology library is selected and select OK.

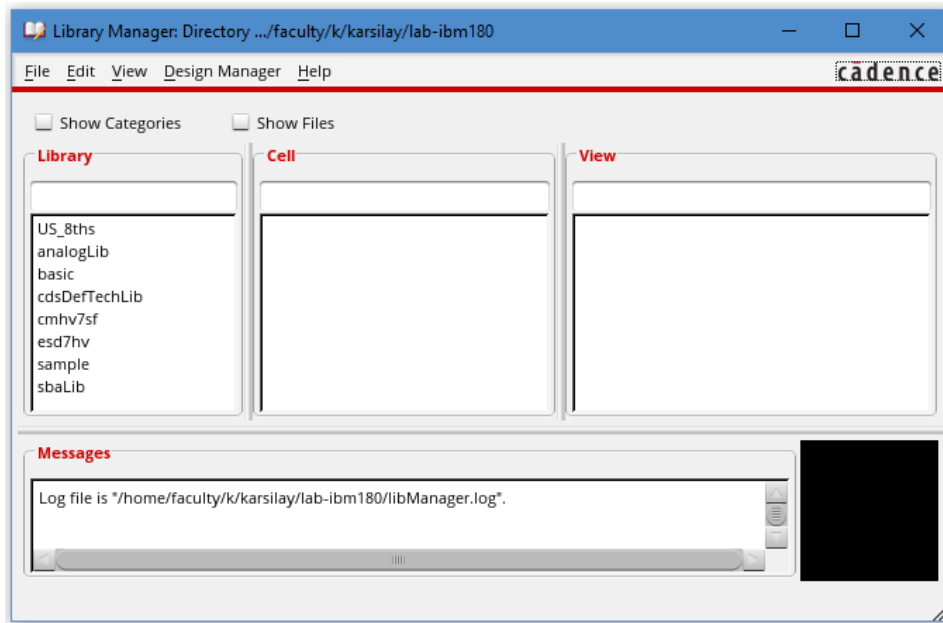


Figure 1-4: The Library Manager Window

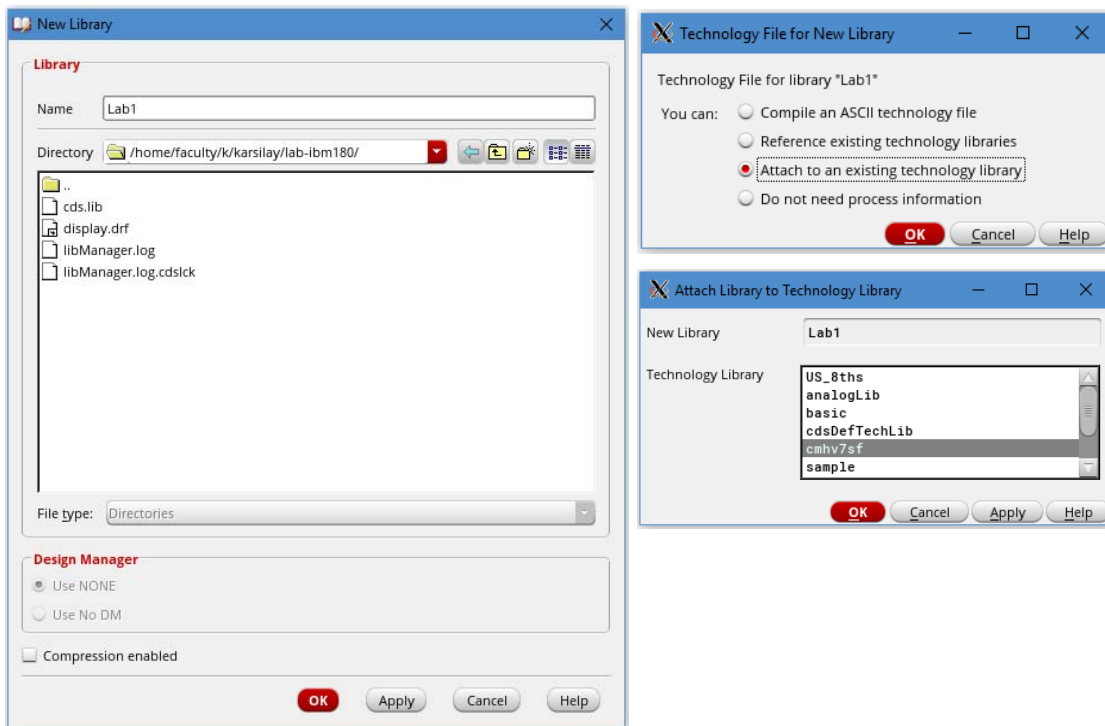


Figure 1-5: Creating a Library and Attaching a Technology Library

Creating a Cell

The first circuit we will design is a simple inverter. Select the library you want to put the cell into by clicking on it to highlight it, in this case "Lab1", and then *File*→*New*→*Cell View*. Name your cell Inv1. The application you want to use here is Schematics L as seen in Figure 1-6. After selecting OK on the "New File" tab and OK on the next popup window, the schematic window opens.

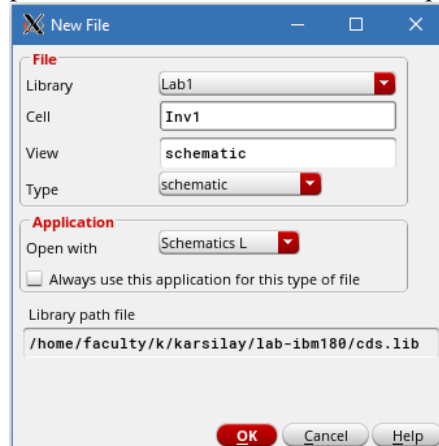


Figure 1-6: Creating a New Cell View

Working with the Schematic Editor

We wish to add two transistors so that we can make an inverter. To do this we need to add an instance. You can do this by either clicking *Create*→*Instance* or by pressing the "i" hotkey on the keyboard. A window titled "Component Browser" should pop up. Hit the "Browse" button, and make sure the library **cmhv7sf** is selected. Select **nfetx** and make sure **symbol** is highlighted. A window with all the FET parameters should pop up. The parameters may be edited if desired, but for the purpose of lab 1 they will not be edited for the NFET. Next, click "hide" and place the NFET on the schematic. Go back to the Component Browser and select **pfetx** and again make sure **symbol** is highlighted. Next, the components need to be connected together by wires. You can select *Add*→*Wire* or use the "w" hotkey. The parameters of the PFET need to be changed if they were not changed earlier. To change the parameters of a device use *Edit*→*Properties*→*Objects* or use the "q" hotkey after selecting the device. In order to compensate for the lower mobility in the PMOS transistor, the width of the PMOS transistor needs to be changed from 500 nm to 1 μm . This can be done by methods previously mentioned or by selecting the element and editing its properties in the Property Editor Window in the lower left of the schematic window. Next, add sources to the circuit by adding an instance and browsing the "analogLib" library. The power supply and the input voltage sourced need to be added. The voltage for the power supply should be 1.8V and the voltage for the input should be "Vidc" (without the quotes). When all is complete it should resemble Figure 1-7. Also a summary of common schematic editor hotkeys and commands is shown in Table 1-2.

Table 1-2: Common Schematic Editor Commands

w	Draw wire
i	Add instance
delete	Will delete anything that is clicked
esc	Will return the curser to its normal state
r	Rotate element
m	Move element
f	Zoom fit

c	Copy element
u	Undo
Ctrl-z	Zoom out
Ctrl-d	Deselect everything
Right click and drag	Will zoom in on drawn region
l	Create label

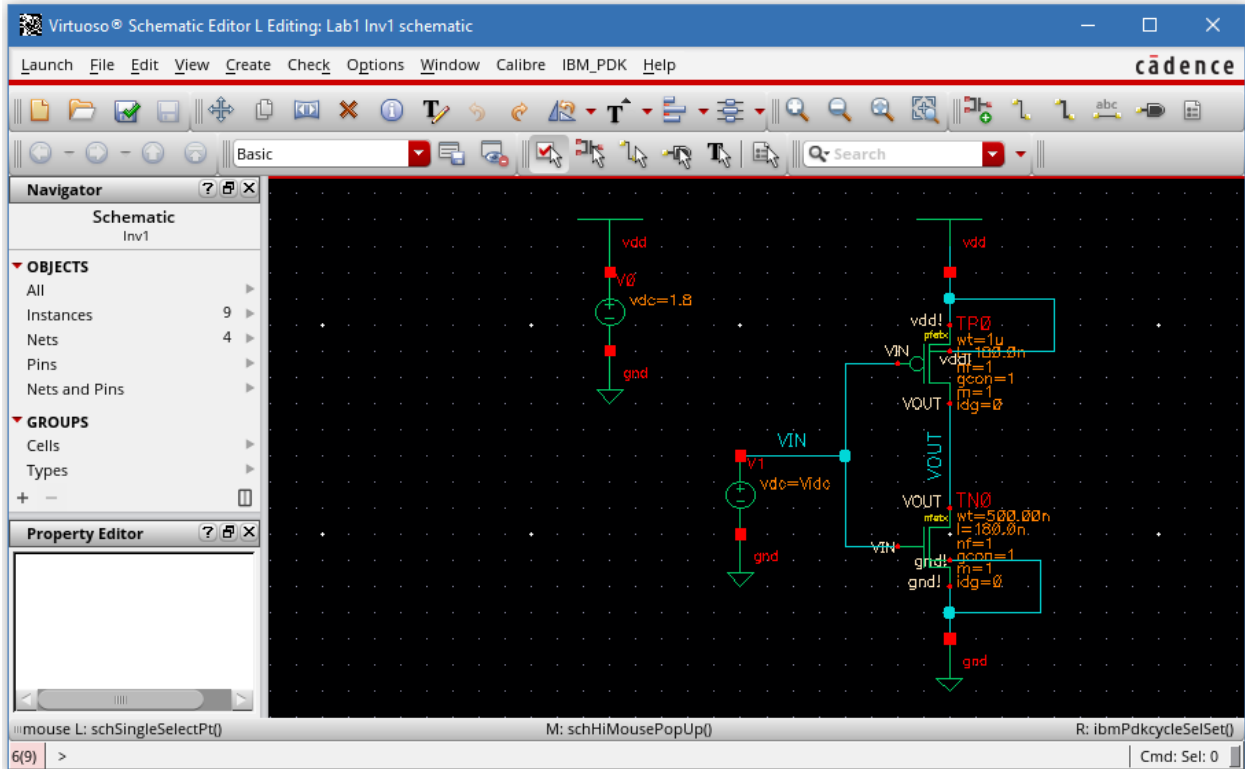


Figure 1-7: Inverter Schematic with Added Sources

Simulating a Schematic

We want to perform a DC sweep of the input voltage "Vdc" from 0V to 1.8V. From the schematic window select *Launch*→*ADE L*. Click OK on the popup window and the ADE L window should appear. Next select *Variables*→*Copy from Cellview*. The variable "Vdc" should appear under the design variables sub window. In the sub window there is nothing under the field "Value" any arbitrary number is needed for the simulation to work, just click the empty box and add "0". Next, go to *Analysis*→*Choose*→<select dc>→<check box "save dc operating point">→<check box "component parameter">→*Select Component*→<click the voltage source labeled "Vdc">→<double click the "DC" option>→<set start to 0 and stop to 1.8>→<click OK>.

Next, we need to tell ADE L which nets to plot. Go to *Outputs*→*To Be Saved*→*Select On Design*→<select the target node>. This process can be repeated with the input node, just remember to click the wire for voltage because clicking a node will give you its current. Because voltage is desired, wires should be selected not nodes. Next, go back to the ADE L window and <check the boxes for "plot" and "save" under the "Outputs" section of the window>. Once this stage is reached the ADE L window should look like Figure 1-8. Next, <click the green play button to the right of the window>. The output plot after clicking the green play button should resemble Figure 1-9.

Alternatively, you may skip the paragraph above, and just <click the green play button to the right of the window> (or click on *Simulation*→*Netlist and Run* from the ADE L menu). After simulation is complete, you may click on the ADE L menu item *Results*→*Direct Plot* →*DC*, then select the wires on the schematic window, and press ESC. You will see the same plot window in Figure 1-9.

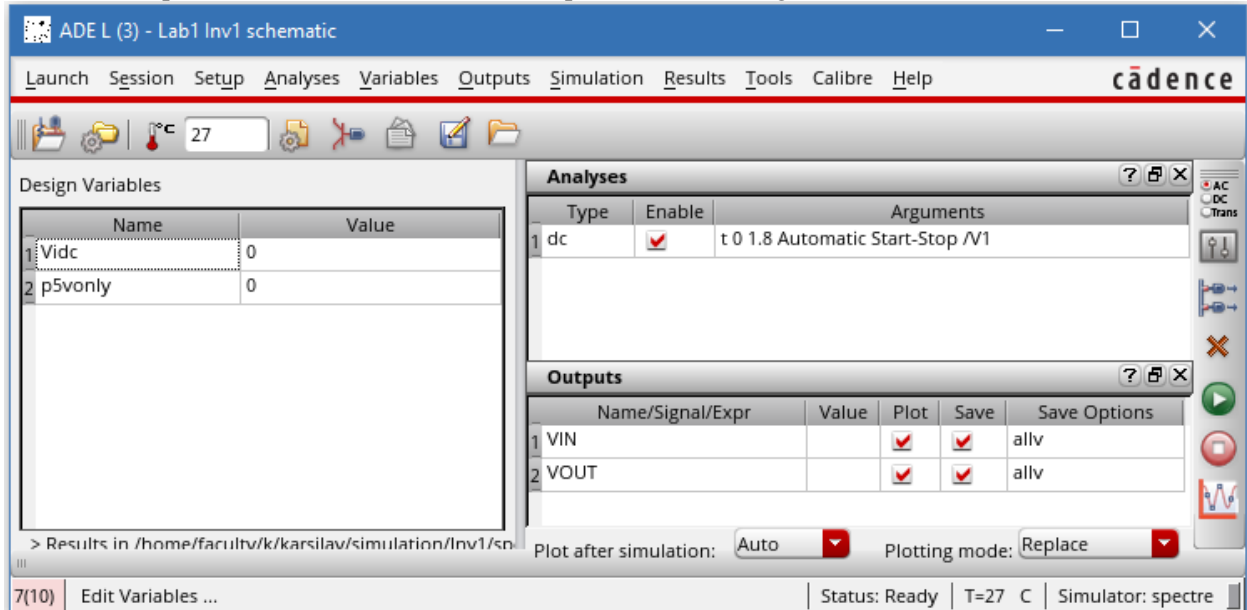


Figure 1-8: The ADE L Window after the Setup Process is Complete

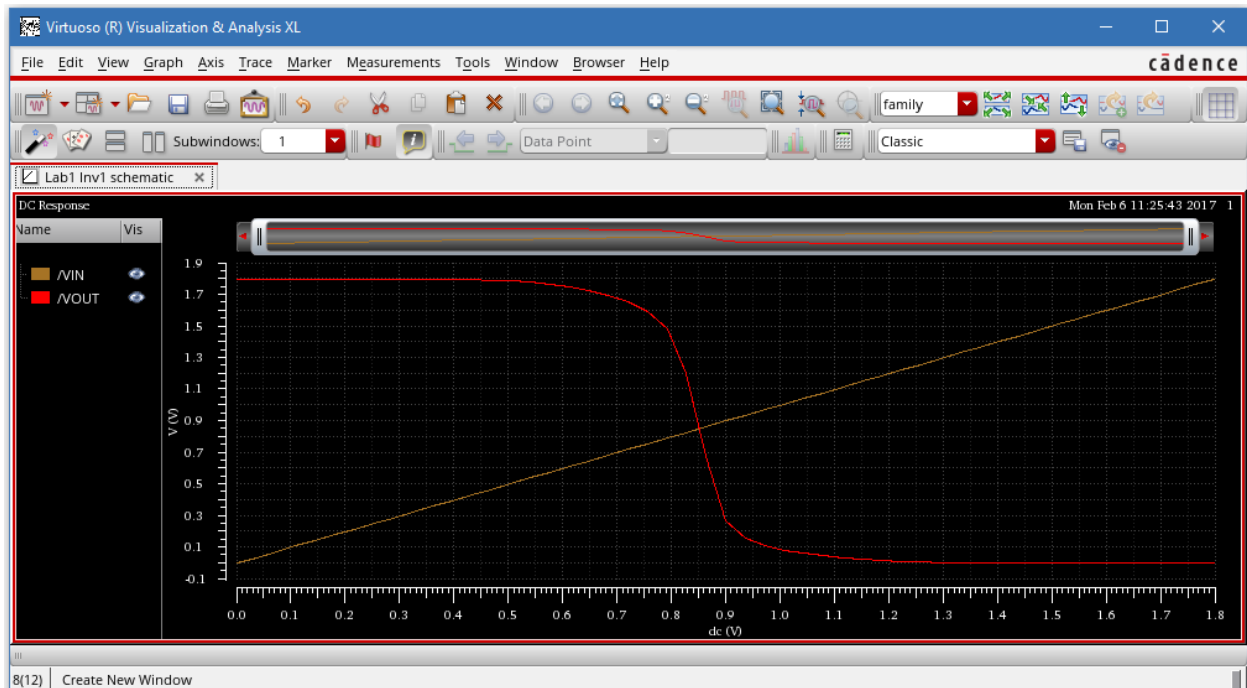


Figure 1-9: The Output Plot of the Schematic Simulation of the Inverter

Transistor Operation

MOS transistors are the fundamental devices of CMOS integrated circuits. The schematic symbols for an NMOS and PMOS transistor are illustrated in Figure 1-10 and Figure 1-11, respectively.

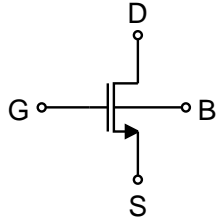


Figure 1-10: NMOS Transistor

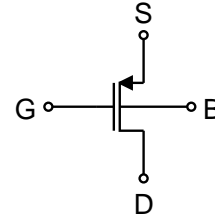


Figure 1-11: PMOS Transistor

A cross sectional view of an NMOS transistor is shown in Figure 1-12. When the potential difference between the source (S) and the Drain (D) is small (~ 0 V), and a large potential ($> V_{T0}$) is applied between the gate (G) and source, the transistor will be operating in the linear or ohmic region. The positive gate potential causes electrons to gather below the surface of the substrate near the gate in a process called "inversion". This region of mobile charge forms a "channel" between the source and drain. The amount of charge is a function of the gate capacitance (C_{ox}) and the gate-to-source overdrive voltage:

$$Q_m = C_{ox}(V_{GS} - V_{T0})$$

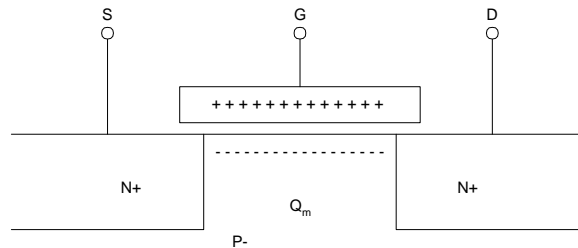


Figure 1-12: Cross-Sectional View of an NMOS Transistor

The term V_{T0} is the threshold voltage. When the gate-to-source voltage (V_{GS}) exceeds this value, an inversion region is formed. Before reaching the inversion region, as the gate-to-source voltage is increased, the transistor passes through the accumulation region where holes are repelled from and electrons are attracted to the substrate region under the gate. Immediately before inversion, the transistor reaches the depletion region (weak-inversion) when the gate to source voltage is approximately equal to the threshold voltage. In this region a very small current flows.

In the linear region, the MOSFET acts a voltage controlled resistor. Resistance is determined by V_{GS} , transistor size, and process parameters.

When the drain-to-source voltage (V_{DS}) is increased, the quantity and distribution of mobile charge carriers becomes a function of V_{DS} as well. Now the total charge is given by:

$$Q_m = C_{ox}(V_{GS} - V_T - V_{DS})$$

The threshold voltage (now denoted as V_T) becomes a function of V_{DS} . This distribution of this charge is such that Q_m is greater near the source and less near the drain. To find the channel conductance, the charge must be recast as a function of position $Q_m(y)$ and integrated from the source to drain. Since the charge is a function of V_{DS} , the conductance depends on V_{DS} . The channel current becomes:

$$I_D = \mu_0 C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

or

$$I_D = KP \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

As V_{DS} increases, eventually the drain current saturates, That is, an increase in V_{DS} does not cause an increase in current. The saturation voltage depends on V_{GS} and is given by:

$$V_{DS(sat)} = V_{GS} - V_T$$

The equation of the drain current becomes:

$$I_D = \frac{1}{2} KP \frac{W}{L} (V_{GS} - V_T)^2$$

At this point the transistor is operating in the saturation region. This region is commonly used for amplification applications. In saturation, I_D actually depends weakly on V_{DS} with the parameter λ . Also, the threshold voltage depends on the bulk-to-source voltage (V_{BS}) through the parameter γ . A better equation for the MOSFET (that includes the effects of V_{BS}) in saturation is given by:

$$I_D = \frac{1}{2} KP \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

When V_{GS} is less than the threshold voltage, the channel also conducts current. This region of operation is called weak-inversion or sub-threshold conduction. It is characterized by an exponential relationship between V_{GS} and I_D . Also, when V_{GS} becomes very large the charge carrier's velocity no longer increases with the applied voltage. This region is known as velocity saturation and has an I_D that depends linearly on V_{GS} as opposed to the quadratic relation shown above.

Figure 1-13 is a three-dimensional cross-sectional view of a MOSFET. Notice in the figure the overlap between the gate region and the active regions. The overlap forms parasitic capacitors C_{GS} and C_{GD} .

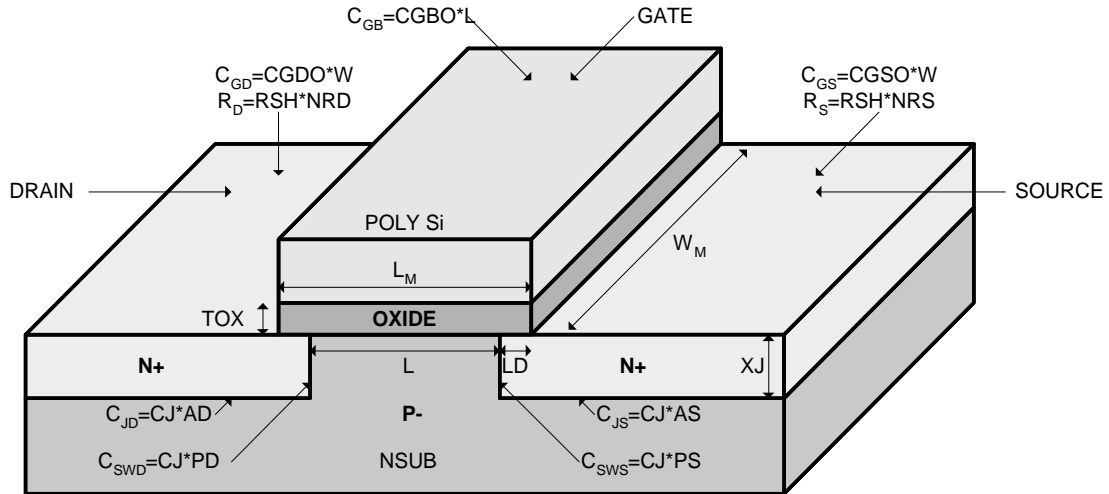


Figure 1-13: Physical Structure of a MOSFET

The reverse-biased junctions between the active regions and the bulk form the parasitic capacitors C_{DB} and C_{SB} . The conductivity of the active regions forms the parasitic resistors R_D and R_S . A schematic symbol with these parasitic elements is illustrated in Figure 1-14.

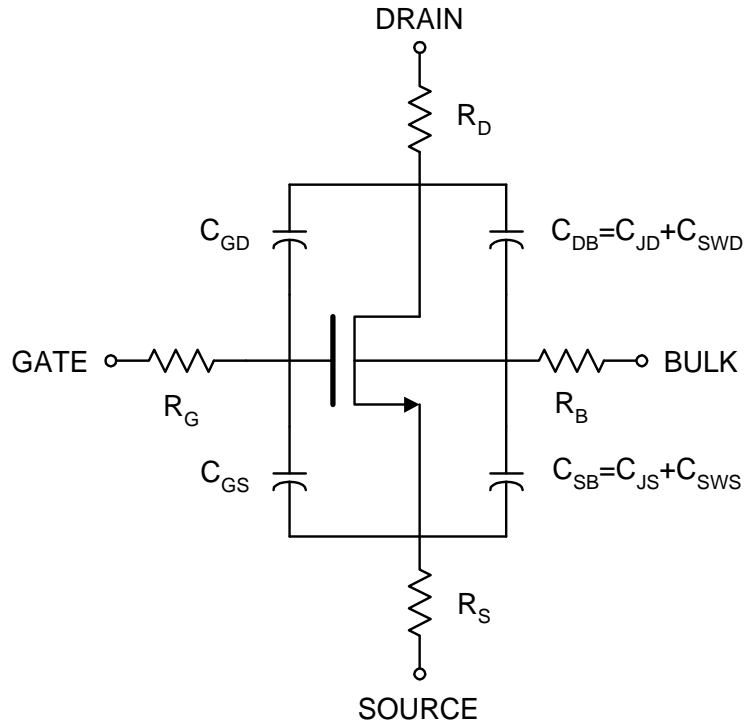


Figure 1-14: MOSFET Parasitic Resistors and Capacitors

Device Characterization

To characterize the MOSFETs so that hand calculations can be done in the future, simulations need to be done to measure K_P , V_{T0} , λ and γ . These parameters will be used in future labs, project and other assignments. We will be performing the calculation of the four parameters on two different device sizes for each of the two types of MOSFETs so that parameter variation may be observed.

The test setups for the NMOS and PMOS transistors are shown in Figure 1-15 and Figure 1-16, which will produce the plots shown in Figure 1-17 and Figure 1-18, respectively, using parametric analysis.

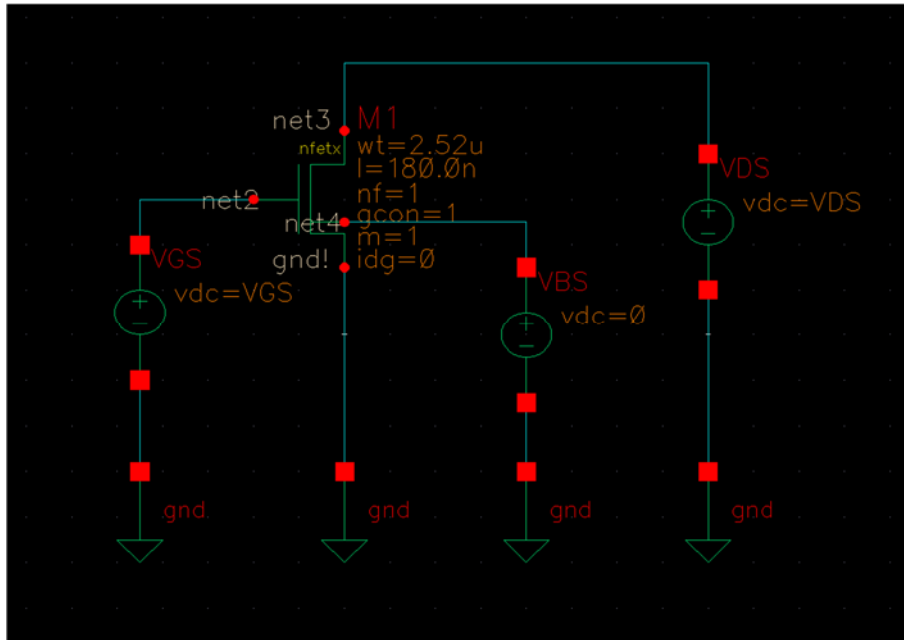


Figure 1-15: Test Setup for the NMOS Transistor

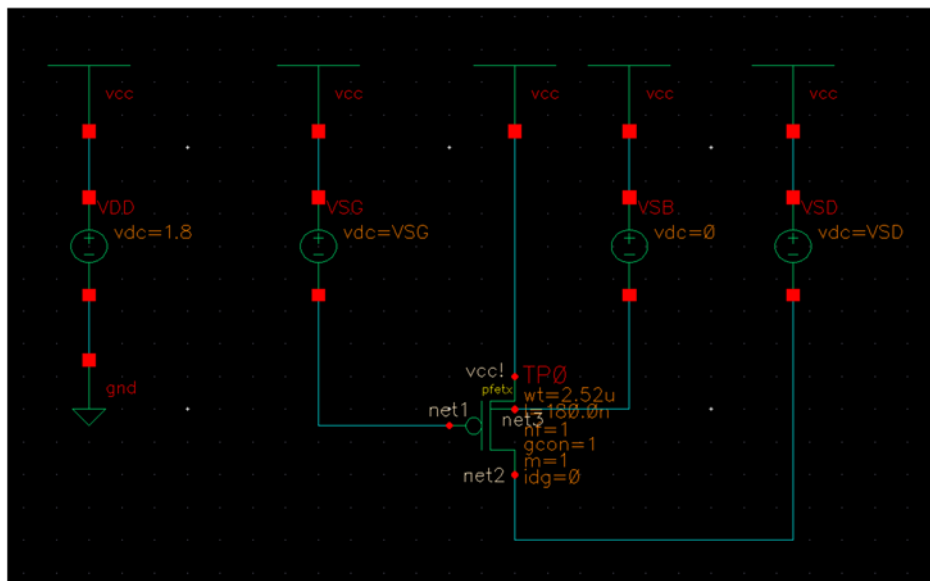


Figure 1-16: Test Setup for the PMOS Transistor

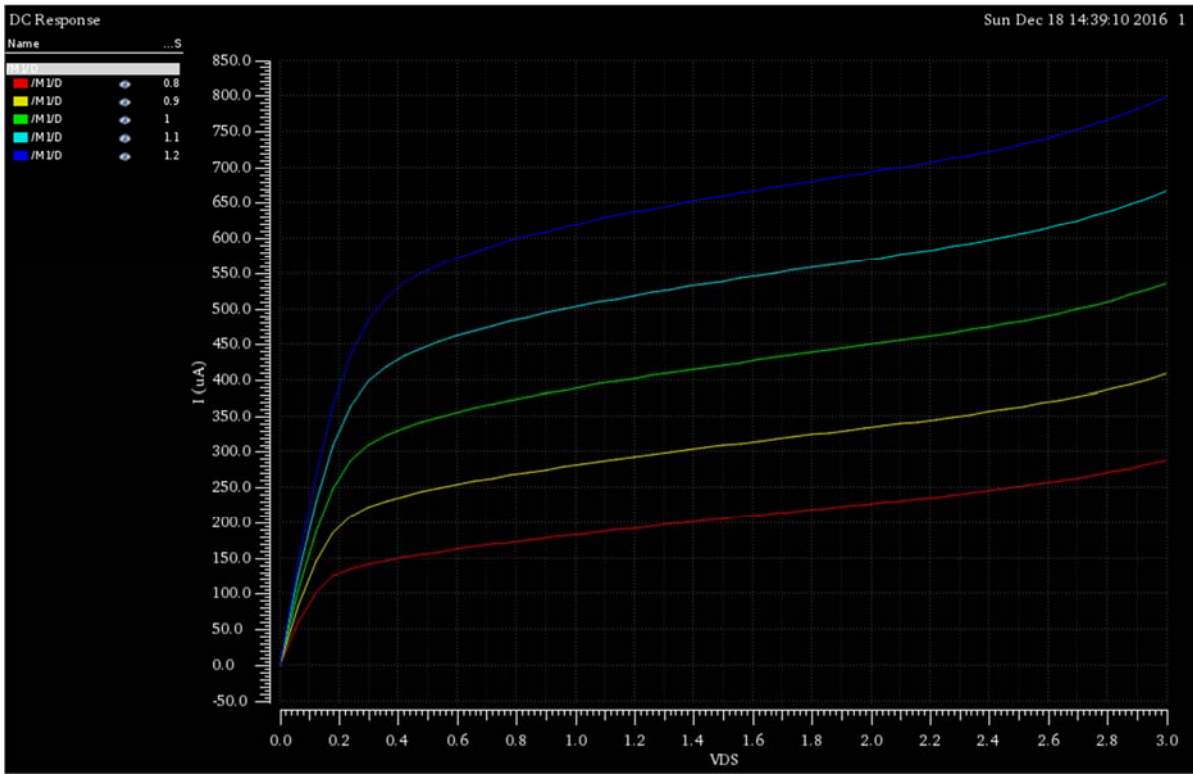


Figure 1-17: Parametric Plot of the NMOS Transistor

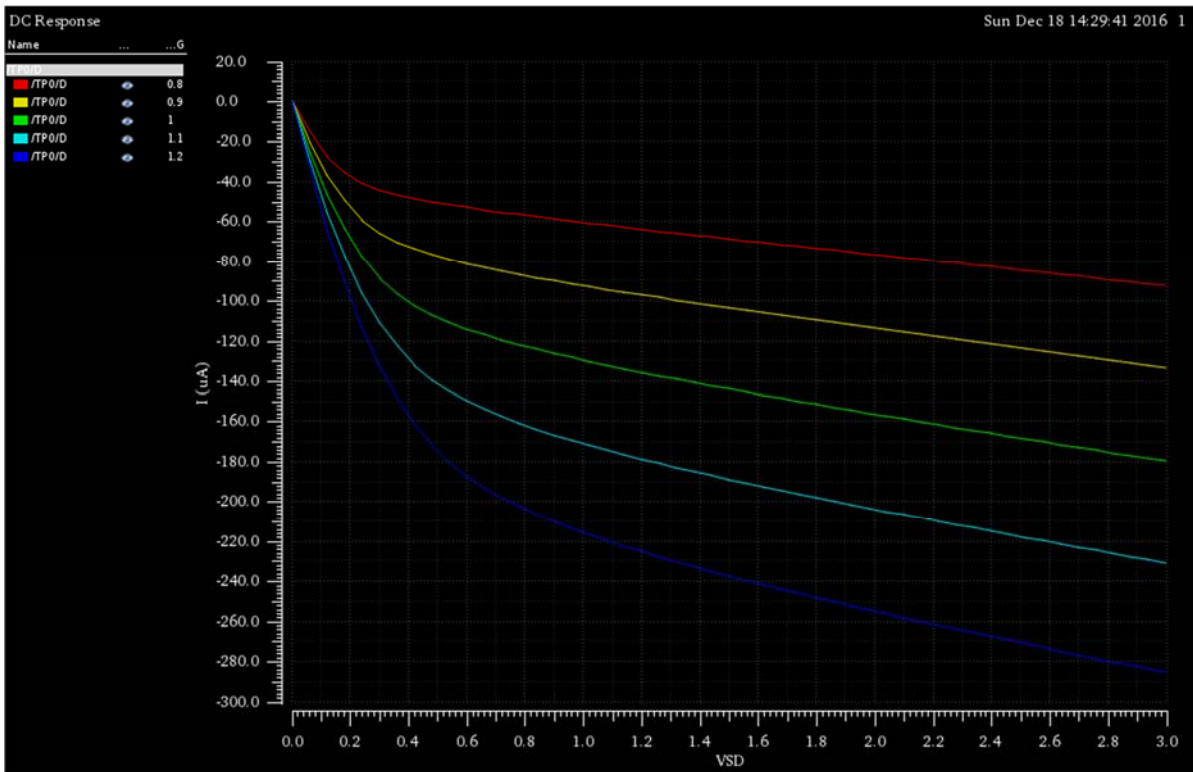


Figure 1-18: Parametric Plot of the PMOS Transistor

Parametric Analysis

Parametric analysis is used when two or more independent variables are present in a single function. We can have the standard X-Y plot of V_{DS} versus I_D with a constant V_{GS} . But we need to plot the same X-Y plot multiple times for each of the discrete V_{GS} values.

To run parametric analysis first go to *Launch*→*ADE L*→*Variables*→*copy from cellview*→<set values of V_{DS} and V_{GS} to "0" in the design variables sub-window>. Next, <choose dc analysis by clicking the button with the words "AC, DC, Trans" on the upper right side of the ADE L window>→<check save dc operating point>→<check design variable under the sweep variable field>→select design variable→<double click V_{DS} in the popup window→set start to "0" and stop to "3"→OK. Next, go to *Outputs*→*to be saved*→select on design→<click the drain node (where the device meets the wire at the red dot to measure current instead of voltage)>. Note that clicking wires gives voltages and clicking nodes gives current. Next, <check the "plot" box in the outputs sub-window>→*Tools*→*Parametric Analysis*.

Once the parametric analysis window (Figure 1-19) is open, <select V_{GS} from the dropdown window under the "Variable" field>→<set "From" to 0.8 and "To" to 1.2>→<set the field "Step Mode" to "Linear Steps" from the dropdown menu>→<set "Step Size" to 100m>. Note that for "Step Size" it will appear as "Total Steps" in the field name but it changes to "Step Size" only after "Linear Steps" is set under "Step Mode" and after you click on the empty box below the "Total Steps" field.

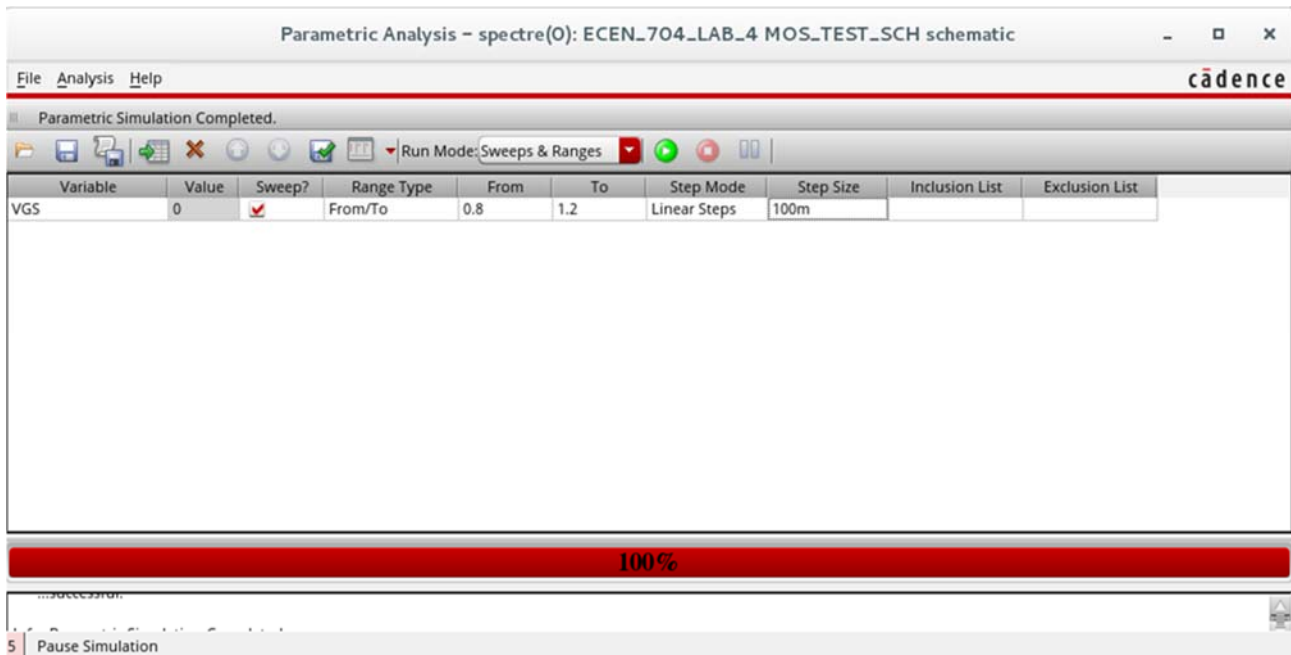


Figure 1-19: The Parametric Analysis Window

Measuring λ

To measure λ you need to do a DC sweep of V_{DS} and plot I_D as shown in Figure 1-17. Each curve represents a different V_{GS} value. Any one of these curves can be used to calculate λ . Make sure that V_{BS} is 0V for this simulation. The formula for calculating λ given two points on the saturation portion of a single curve is:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}}$$

Measuring V_{T0}

V_{T0} can also be obtained from Figure 1-17. Using the saturation portion of two curves with equal V_{DS} then V_{T0} can be calculated as:

$$V_{T0} = \frac{V_{GS1} - V_{GS2} \sqrt{\frac{I_{D1}}{I_{D2}}}}{1 - \sqrt{\frac{I_{D1}}{I_{D2}}}}$$

Measuring KP

Knowing λ and V_{T0} , KP can easily be found from the equation for a MOSFET drain current in the saturation region. A little algebra gives that KP is:

$$KP = \frac{2I_D}{\frac{W}{L} (V_{GS} - V_{T0})^2 (1 + \lambda V_{DS})}$$

Measuring γ

To obtain γ you must first give the transistor a non-zero V_{BS} . Next, calculate the new V_T using the same procedure that you used to obtain V_{T0} where $2\Phi_F = 0.7$ V. γ is given as:

$$\gamma = \frac{V_T - V_{T0}}{\sqrt{|2\Phi_F| + |V_{BS}|} - \sqrt{|2\Phi_F|}}$$

Additional Notes

While in graph mode, you can use the "M" key to insert a marker. The "A" and "B" keys will insert markers as well, except they will give the dx, dy and slope between the two points. The "H" key will generate a horizontal bar, and the "V" key will generate a vertical bar.

Prelab

The prelab exercises are due at the beginning of the lab period. No late work is accepted.

Derive the equations for the four electrical parameters given in the Device Characterization portion of the manual. No computer work is required for the prelab.

Lab Report

1. Turn in printouts of your inverter schematic and DC sweep output plot.
2. Use Cadence to produce I_D versus V_{DS} versus V_{GS} plots similar to Figure 1-17 for transistors of size $1.26 \mu\text{m}/180 \text{ nm}$ and $2.52 \mu\text{m}/180 \text{ nm}$. Sweep V_{GS} from 0.8 V to 1.2 V with 5 steps (100 mV step size).
3. Extract the four electrical parameters (λ , V_{T0} , KP and γ) for both NMOS and PMOS transistors and for both transistor sizes.