ECEN 474/704 Lab 3: Advanced Layout Techniques

Guard Rings

When laying out sensitive analog blocks, we need to help minimize the effect of substrate noise. One way to do this is with a guard ring, which is an array of substrate contacts that is connected to a clean supply (VDD, VSS or ground).

An example of a guard ring is shown in Figure 3-1. This example shows a ring with a single contact. For more isolation, this ring can be made wider with more substrate contacts.

It is also important to note that the PMOS devices have an n-well contact ring surrounding them. This is good practice because it helps to act as an additional guard ring while also minimizing the possibility of latch up between the n-well and substrate.

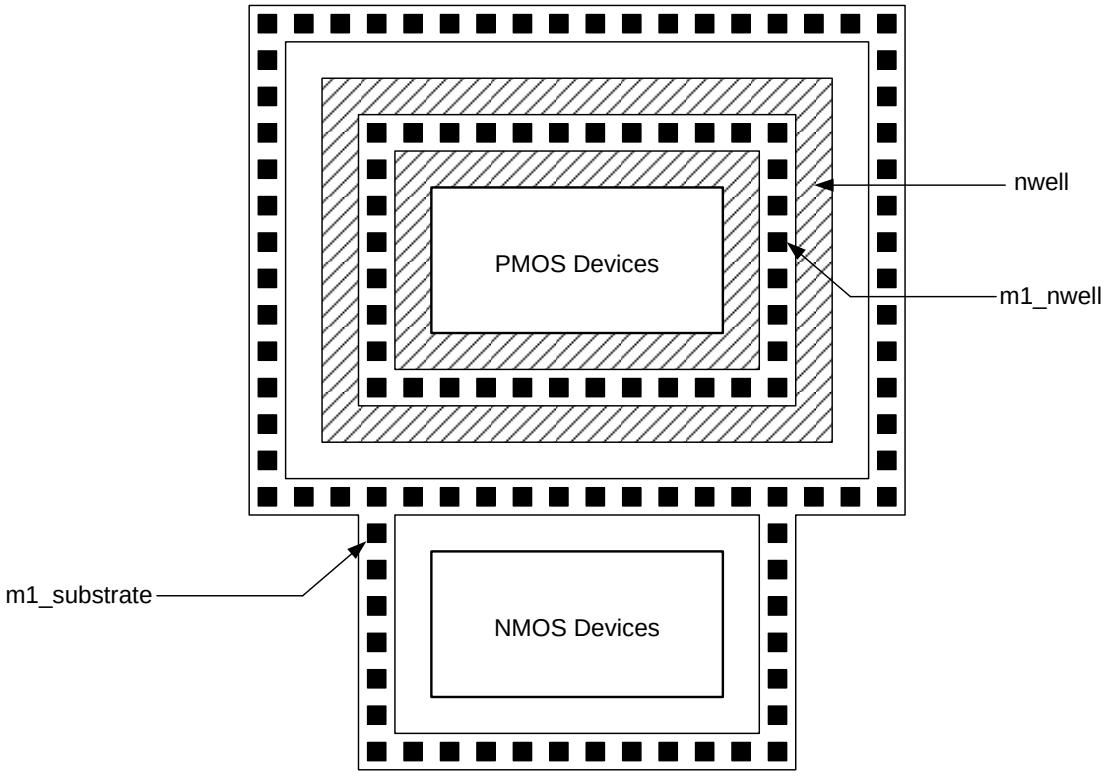

Figure 3-1: Guard Ring Illustration

For this lab, you will design a layout for the two-stage op-amp schematic in Figure 3-2 using good layout techniques with guard rings. Table 3-1 lists the transistor sizes for the op-amp, whereas Figure 3-3 shows a suggested floor plan to use. In this floor plan, each transistor has a finger width of 720 nm. One possible configuration for the placement of the dummy transistors is shown in Figure 3-4.

During the implementation of guard rings, if stacked vias are used, they need to be exactly on top of each other even if they are on the same metal layer (i.e. the "X" in the center should be perfectly aligned with the "X" of the other via to be stacked). Figure 3-5 shows an example of how the guard ring vias should intersect, and Figure 3-6 shows an example of stacked vias from "MT" to "M2". Do not forget to wire your inner most via (the one in the n-well) to the positive power rail and the outermost rings to the negative rail.

Table 3-1: Transistor Sizes

MOSFET	W	L
M1	2.88u	180n
M2	2.88u	180n
M3	5.76u	180n
M4	5.76u	180n
M5	1.44u	180n
M6	2.88u	180n
M7	5.76u	180n
M8	23.04u	180n

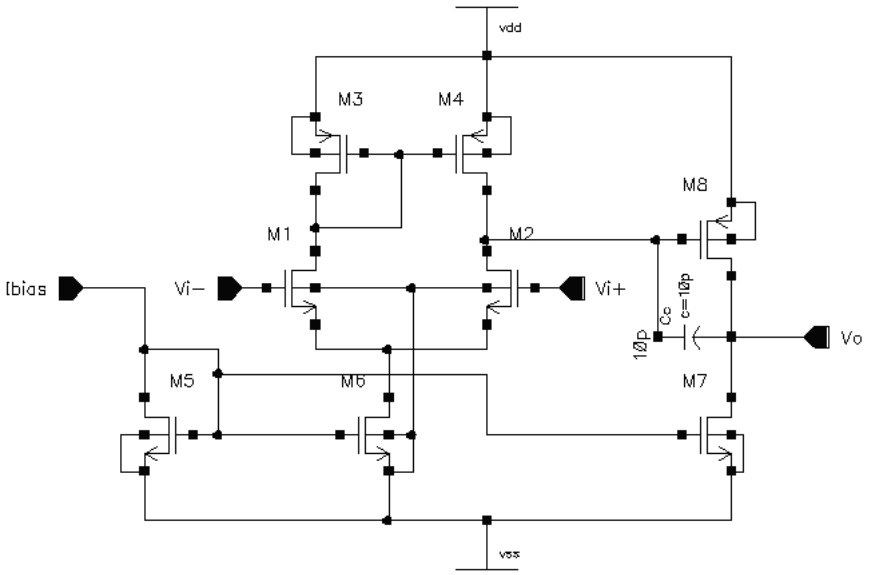

Figure 3-2: Two-Stage Op-Amp

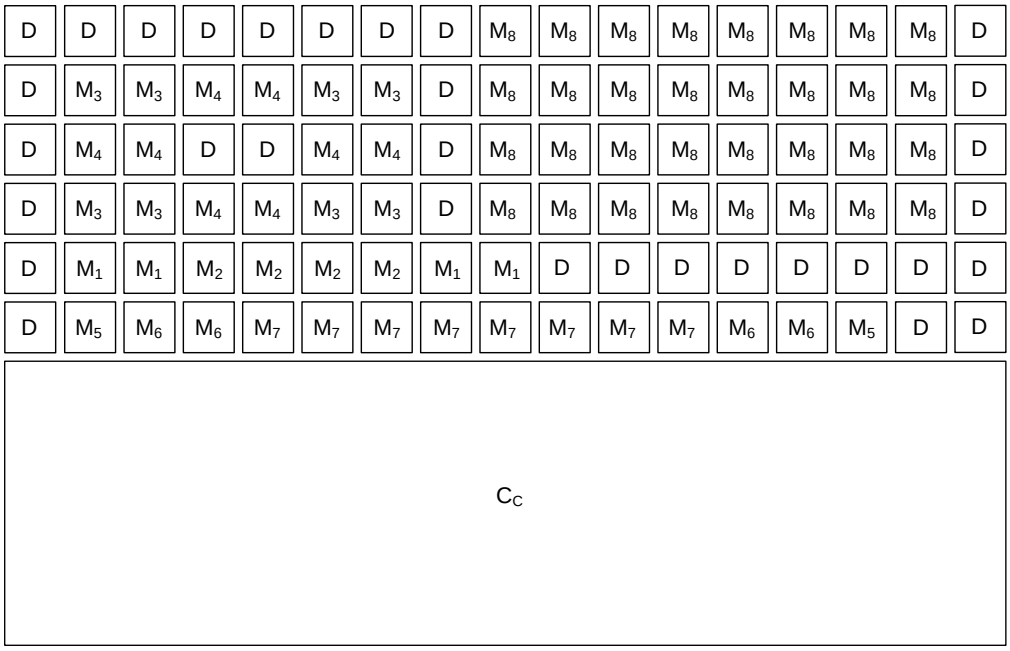

Figure 3-3: Floor Plan for Two-Stage Op-Amp

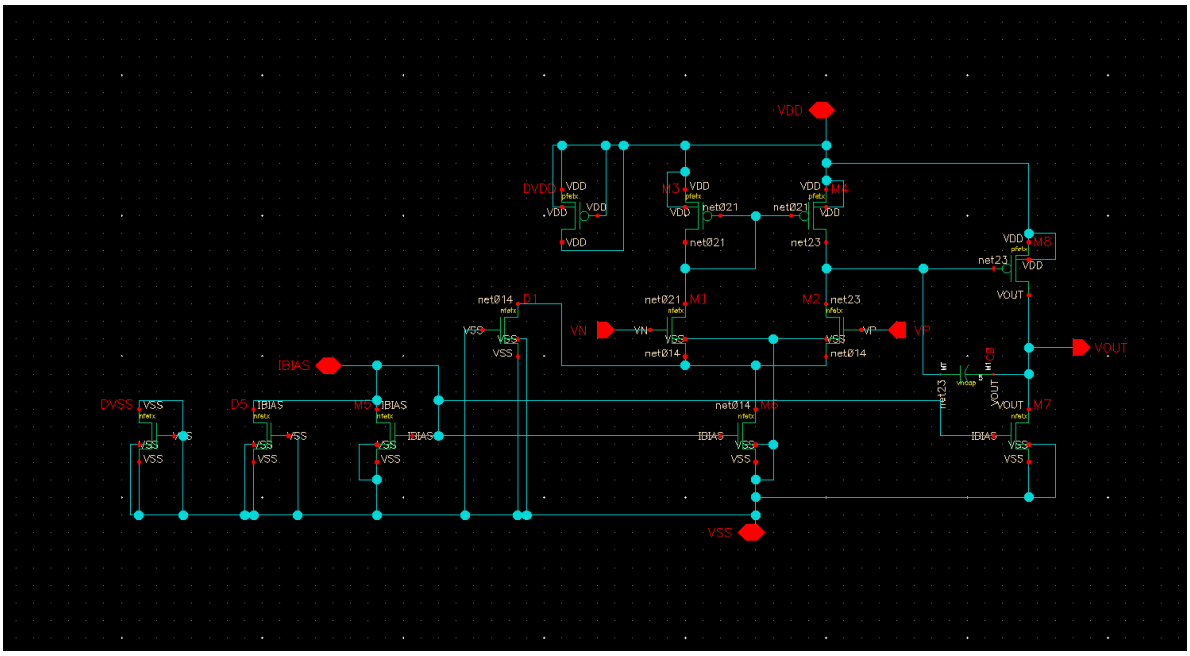

Figure 3-4: Schematic Showing Dummy Transistor Placement

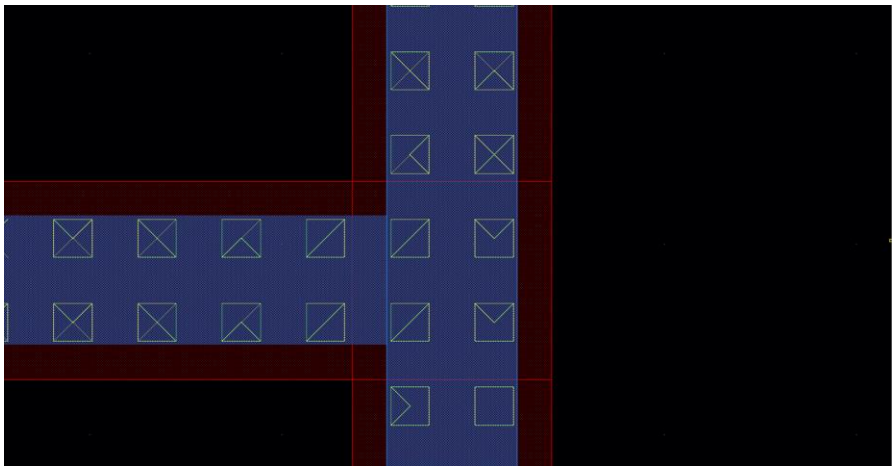

Figure 3-5: Intersection of Guard Rings

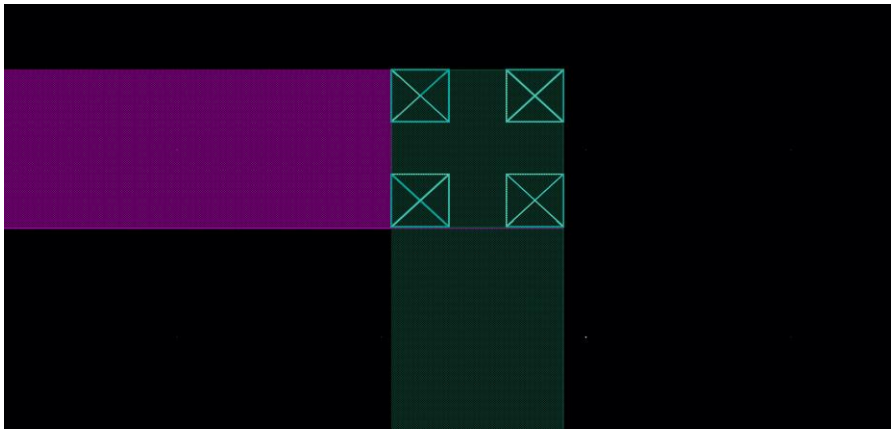

Figure 3-6: Example of Properly Stacked Vias

To implement the capacitor in the layout, select "vncap" from the "cmhv7sf" library, and change the "Backplate" field to "SUB", "Bottom Level Metal" field to "M1" and the "Top Level Metal" to "MT". This will greatly reduce the size of the capacitor needed for the layout. Note that guard rings also need to be implemented for the capacitors.

Prelab

There is no prelab work required for this lab.

Lab Report

1. Schematic printout

2. Layout printout

3. LVS printout showing that layout and schematic match
   (Remember to include the NetID and timestamp in the screen capture.)