

ECEN 474/704 Lab 6: Differential Pairs

Objective

Design, simulate and layout various differential pairs used in different types of differential amplifiers such as operational transconductance amplifiers and operational amplifiers.

Introduction

Differential pairs are used as the input stages of operational amplifiers and operational transconductance amplifiers, common mode feedback circuits, and analog multipliers. As with the other fundamental building blocks, a good understanding of differential pairs is required for successful analog circuit design.

A differential pair consists of two well matched, source-coupled transistors as shown in Figure 6-1. An input voltage between the two gate terminals produces an output current in the drain terminals.

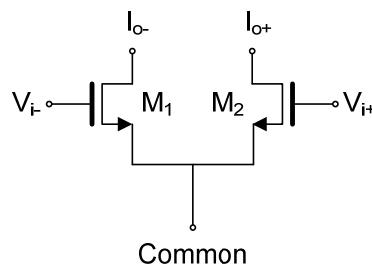


Figure 6-1: Basic Differential Pair

The most common application for a differential pair is the differential amplifier. Figure 6-2 shows the basic differential amplifier. It consists of a differential pair which is biased by the tail current source I_{tail} . Resistor R_{tail} models the output resistance of a real current source. Load resistors R_{D1} and R_{D2} allow the amplifier to develop an output voltage. The output voltage can be differential or single ended. A differential output is developed between the two output terminals, while the single ended output is taken between one output and ground.

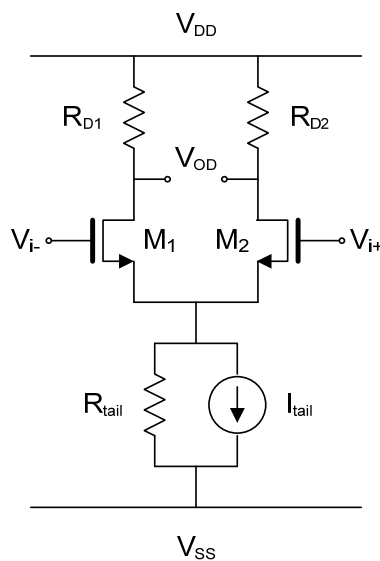


Figure 6-2: Basic Differential Amplifier

The task of the differential amplifier is to amplify the difference between its two input signals. The signals can be decomposed into two components. The first component is called the differential mode voltage V_{DM} and is given by:

$$V_{DM} = V_1 - V_2$$

The second component is called the common mode voltage V_{CM} and is given by:

$$V_{CM} = \frac{V_1 + V_2}{2}$$

Assuming M_1 and M_2 are in saturation, neglecting the effects channel length modulation, and assuming perfectly matched transistors, the large signal characteristics can be analyzed as follows:

$$V_{DM} = V_{G1} - V_{G2} = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_{D1}}{\beta_1}} - \sqrt{\frac{2I_{D2}}{\beta_2}}$$

$$I_{tail} = I_{D1} + I_{D2}$$

where $\beta = KP_N (W/L)$. Assuming $\beta = \beta_1 = \beta_2$ and combining both equations, we can obtain two equations describing the drain currents:

$$I_{D1} = \frac{I_{tail}}{2} + \frac{I_{tail}}{2} \sqrt{\frac{\beta V_{DM}^2}{I_{tail}} - \frac{\beta V_{DM}^4}{4I_{tail}^2}}$$

$$I_{D2} = \frac{I_{tail}}{2} - \frac{I_{tail}}{2} \sqrt{\frac{\beta V_{DM}^2}{I_{tail}} - \frac{\beta V_{DM}^4}{4I_{tail}^2}}$$

These equations are only valid when M_1 and M_2 in saturation and the following relationship is satisfied:

$$|V_{DM}| \leq \sqrt{\frac{2I_{tail}}{\beta}}$$

This means that when V_{DM} is greater than or equal to the above expression, only one of the transistors is conducting and the other is off. Figure 6-3 illustrates the large signal effects as previously described.

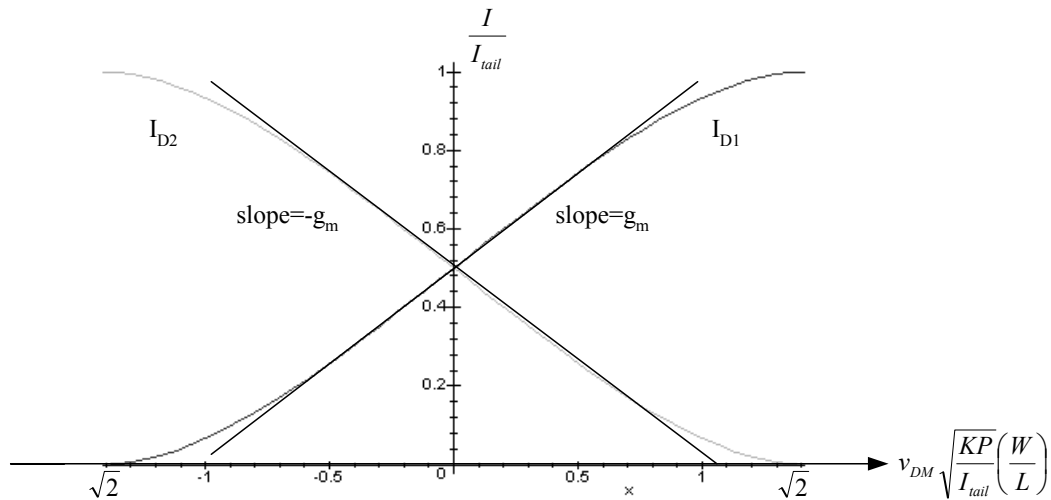


Figure 6-3: Normalized Large Signal Transconductance Characteristic of a MOS Differential Amplifier

The desired behavior of the differential amplifier is to amplify the differential mode voltage and attenuate the common mode voltage. The differential gain A_{DM} of an amplifier with a differential output is defined as:

$$A_{DM} = \frac{V_{OD}}{V_{DM}}$$

where V_{OD} is the differential output voltage. For a single-ended differential amplifier, the gain is defined as:

$$A_{DM} = \frac{V_{OS}}{V_{DM}}$$

where V_{OS} is the single ended output voltage. For an amplifier with a differential output, the common mode gain is defined as:

$$A_{CM} = \frac{V_{OD}}{V_{CM}}$$

and for an amplifier with a single ended output, the common mode gain is defined as:

$$A_{CM} = \frac{V_{OS}}{V_{CM}}$$

For a symmetrical amplifier such as the fully differential amplifier, that is an amplifier with a differential output and a differential input, the common mode voltage gain will be zero if the differential pair is perfectly matched. Due to mismatches in the differential pair or in the loads, a common mode input voltage can cause a differential output voltage. A figure of merit for differential amplifiers is the common mode rejection ratio (CMRR). The CMRR is defined as the ratio of the differential gain and common mode gain:

$$CMRR = 20 \log_{10} \left(\left| \frac{A_{DM}}{A_{CM}} \right| \right)$$

The input common mode voltage is limited in magnitude. The inputs must not force any of the transistors out of saturation. The limitation on the common mode voltage creates a common mode voltage range for the amplifier. When the common mode voltage increases above the upper limit, the transistors in the differential pair will leave the saturation region and enter the linear region. If the common mode voltage decreases below the lower limit, then the transistors in the tail current source will be forced out of saturation. The common mode voltage range can be found by considering the saturation voltages for differential pair transistors and current source transistors. Remember, for a transistor to be in saturation the overdrive voltage must not exceed the saturation voltage:

$$V_{DS,sat} = V_{GS} - V_{T0} = \sqrt{\frac{2I_D}{KP_N \frac{W}{L}}}$$

The output voltage range is also limited. For a single ended amplifier with symmetrical power supplies, the magnitude of the output signal is limited to the supply rails:

$$V_{OS} \leq |V_{DD}|$$

However, for fully differential amplifiers the output signal can be twice this amplitude. Each output can swing to a supply rail, giving a differential output voltage that is twice as large as either rail. As with all amplifiers, another limit on the output voltage swing is the allowable distortion. An output signal swing

which comes within 200 mV of the supply rails may have 10% THD. And a signal which comes within 500 mV may have only 1% THD in the same circuit. The output voltage range is dictated by the distortion requirement.

The input-output characteristic curves of the differential amplifier are shown in Figure 6-4. The region where the input is approximately zero volts is linear. The size of the linear region is determined by the transistor sizes. Decreasing the transistor sizes will decrease the transconductance and increase the size of the linear region.

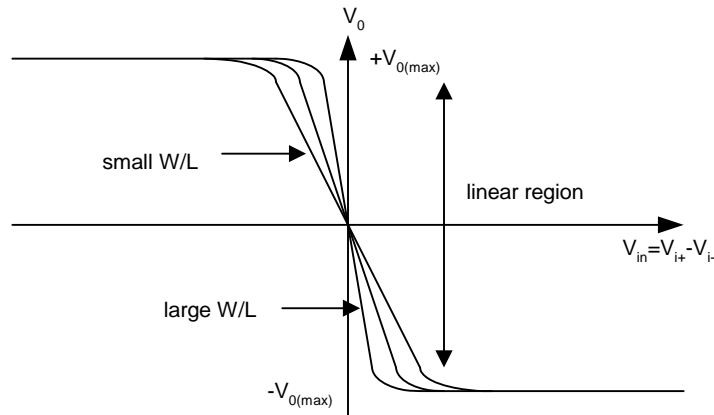


Figure 6-4: Input-Output Characteristic Curves for a Differential Amplifier

The amplifier also has an input and output impedance. The differential input resistance and the common mode input resistance are large for MOSFET differential amplifiers. The differential input resistance is the resistance between the two input terminals. The common mode input resistance is the resistance measured between the two interconnected inputs and ground.

The output impedance can also be measured in two different ways. For fully differential amplifiers, the differential output resistance is the resistance between the two output terminals. For single ended amplifiers, the common mode output resistance is the resistance measured between the output and ground.

Another figure of merit for the differential amplifier is its power supply rejection ratio (PSRR). This ratio indicates the effect of power supply variations or noise on the output voltage. For fully differential amplifiers with perfect matching in the differential pair and load, the PSRR is zero. PSRR is given by:

$$PSRR^+ = 20 \log_{10} \left(\left| \frac{A_{DM}}{V_o/V_{DD}} \right| \right) \qquad PSRR^- = 20 \log_{10} \left(\left| \frac{A_{DM}}{V_o/V_{SS}} \right| \right)$$

The slew rate is a measure of how quickly the output of the differential amplifier can change in response to an instantaneous rail-to-rail (large signal) change in the input voltage.

Due to process variations, the differential pair will not be perfectly matched. As a result, for equal input voltages, the drain currents will not be equal. Also, if the load is asymmetrical, then a non-zero output voltage will exist. The voltage at the input which forces the output voltage to zero is called the input offset voltage.

Common-Mode Voltage Range:

As mentioned previously, the common-mode voltage range is the range of input voltages which keep the current source and active load transistors in saturation. The common-mode voltage range is determined by the sizes of the transistors. To increase the common-mode voltage range, the sizes of the transistors must be increased. The common-mode voltage range is given by:

$$V_{SS} + \sqrt{\frac{2I_{tail}}{KP_N \left(\frac{W}{L}\right)_{3,4}}} + \sqrt{\frac{I_{tail}}{KP_N \left(\frac{W}{L}\right)_{1,2}}} + V_{TN} < V_{in(CM)} < V_{DD} - \sqrt{\frac{I_{tail}}{KP_P \left(\frac{W}{L}\right)_{5,6}}} - V_{TP} + V_{TN}$$

Common-Mode Gain:

To design for common mode, we can no longer assume that there exists an AC signal ground at the source of M_1 and M_2 . This current source must be substituted by a resistor of value equal to the output resistance of the current mirror. To help in the development of the design equations, Figure 6-6 is used.

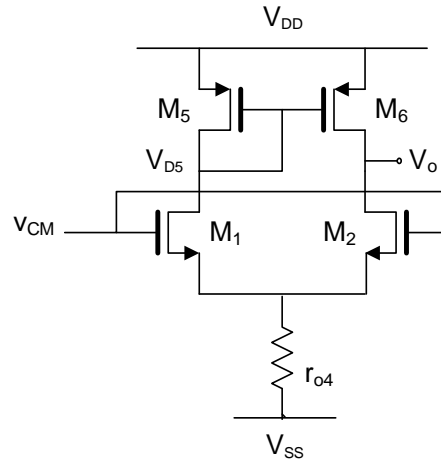


Figure 6-6: Differential Amplifier Used to Determine CMRR

From this figure, the voltage gain from V_{CM} to V_{D5} can be found as:

$$\frac{V_{D5}}{V_{CM}} \approx \frac{-\frac{1}{g_{m5}}}{2r_{o4} + \frac{1}{g_{m1}}} \approx -\frac{1}{2r_{o4}g_{m5}}$$

Assuming perfect matching between M_1 & M_2 , and M_5 & M_6 , it can be shown that $V_o = V_{D5}$. Therefore, the common-mode gain is given by:

$$A_{CM} = \frac{V_o}{V_{CM}} = -\frac{1}{2r_{o4}g_{m5}}$$

As can be seen from this equation, the CMRR can be improved by increasing the output impedance of the tail current source:

$$CMRR = 20 \log_{10} \left(\left| \frac{A_{DM}}{A_{CM}} \right| \right) = 20 \log_{10} (|g_{m1}(r_{o2} || r_{o6})2r_{o4}g_{m5}|)$$

Simple Differential Amplifier with Cascode Current Mirror as the Active Load and Tail Current

The second differential amplifier is shown in Figure 6-7. This circuit utilizes low-voltage cascode current mirrors as the tail current source and the active load. The design equations for this structure are the same as the previous structure except the output impedance of the amplifier and current source are now larger. This will increase differential mode gain while decreasing common mode gain, thus a vastly improved CMRR. The main drawback of this circuit is a reduced input common mode range and output swing.

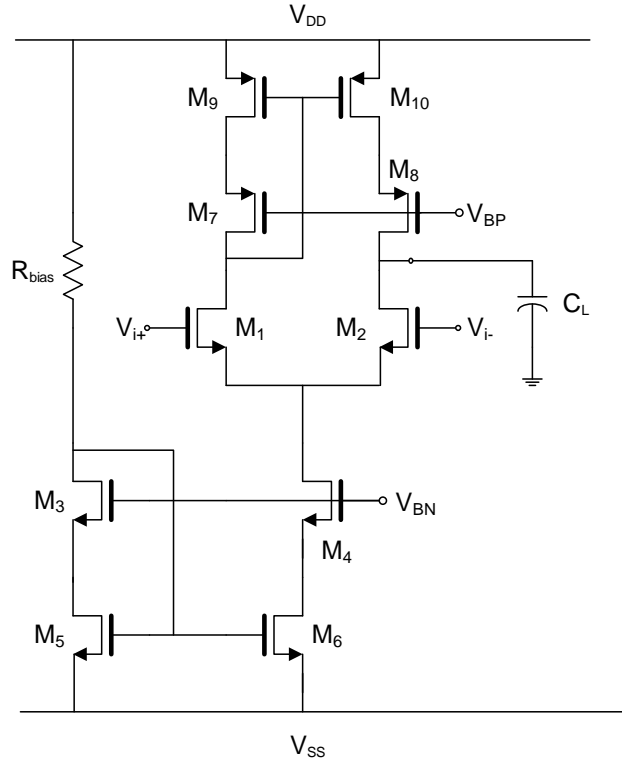


Figure 6-7: Differential Amplifier with Cascode Current Mirror as the Active Load and Tail Current

Differential Gain:

The differential gain of this circuit is given by:

$$A_{DM} = G_m R_{out} = g_{m1} (r_{o2} || (r_{o8} + r_{o10} + g_{m8} r_{o8} r_{o10})) \approx g_{m1} r_{o2}$$

Slew Rate:

The biasing current and the amount of load capacitance determine the slew rate (SR), which is given by:

$$SR = \frac{I_{tail}}{C_L}$$

Gain-Bandwidth Product and Dominant Pole:

Since the output node is a high impedance node, the dominant pole is located at:

$$p_1 = \frac{1}{R_{out} C_L}$$

The gain-bandwidth product is given by:

$$GBW = A_{DM}p_1 = \frac{G_m R_{out}}{R_{out} C_L} = \frac{g_{m1}}{C_L}$$

Common Mode Voltage Range:

The common mode voltage range for this differential amplifier is given by:

$$V_{in(CM)} > V_{SS} + \sqrt{\frac{2I_{tail}}{KP_N \left(\frac{W}{L}\right)_6}} + \sqrt{\frac{2I_{tail}}{KP_N \left(\frac{W}{L}\right)_4}} + \sqrt{\frac{I_{tail}}{KP_N \left(\frac{W}{L}\right)_1}} + V_{TN1}$$

$$V_{in(CM)} < V_{DD} - \left(\sqrt{\frac{I_{tail}}{KP_P \left(\frac{W}{L}\right)_9}} + |V_{TP9}| \right) + V_{TN1}$$

Common-Mode Gain:

The common-mode gain can be expressed as:

$$A_{CM} \approx -\frac{1}{2R_{SS}g_{m9}} \quad , \quad R_{SS} = r_{04} + r_{06} + g_{m4}r_{04}r_{06}$$

Therefore, the CMRR can be found as:

$$CMRR = 20 \log_{10} \left(\left| \frac{A_{DM}}{A_{CM}} \right| \right) \approx 20 \log_{10} (2g_{m1}g_{m4}g_{m9}r_{02}r_{04}r_{06})$$

Operating Region of Transistors in Cadence

Cadence has a function that can test a transistor's region of operation. Testing transistors' regions of operation versus a DC sweep of one parameter can be very useful especially for differential amplifier design.

In this example we will be testing the regions of operation of the transistors in an inverter. The first step is to establish a parameter (the input voltage source in this case) and run a DC sweep of the parameter. Then you will need to run a parametric sweep. For our example we select the same variable that was used for the DC sweep for the "Variable" field, then we will enter the sweep range by setting the "To" and "From" fields to -3 V and 3 V.

Now we're ready to plot the region of operation. Go to *Tools* → *Calculator* → <select "op"> → <select the transistor to test> → <select "Region" from the drop down menu> → *plot*. Note that when you select the transistor, the selection window may disappear, it only goes down to the task bar, just click it to pull it up again and then select "Region" as previously instructed. Once your plot has been generated, it should resemble Figure 6-8. The plot shows a waveform that is at a constant number for a specific range. The values and the corresponding regions of operation are described in Table 6-1.

Table 6-1: Values for Regions of Operation

0	Cutoff
1	Triode
2	Saturation
3	Sub-Threshold
4	Breakdown

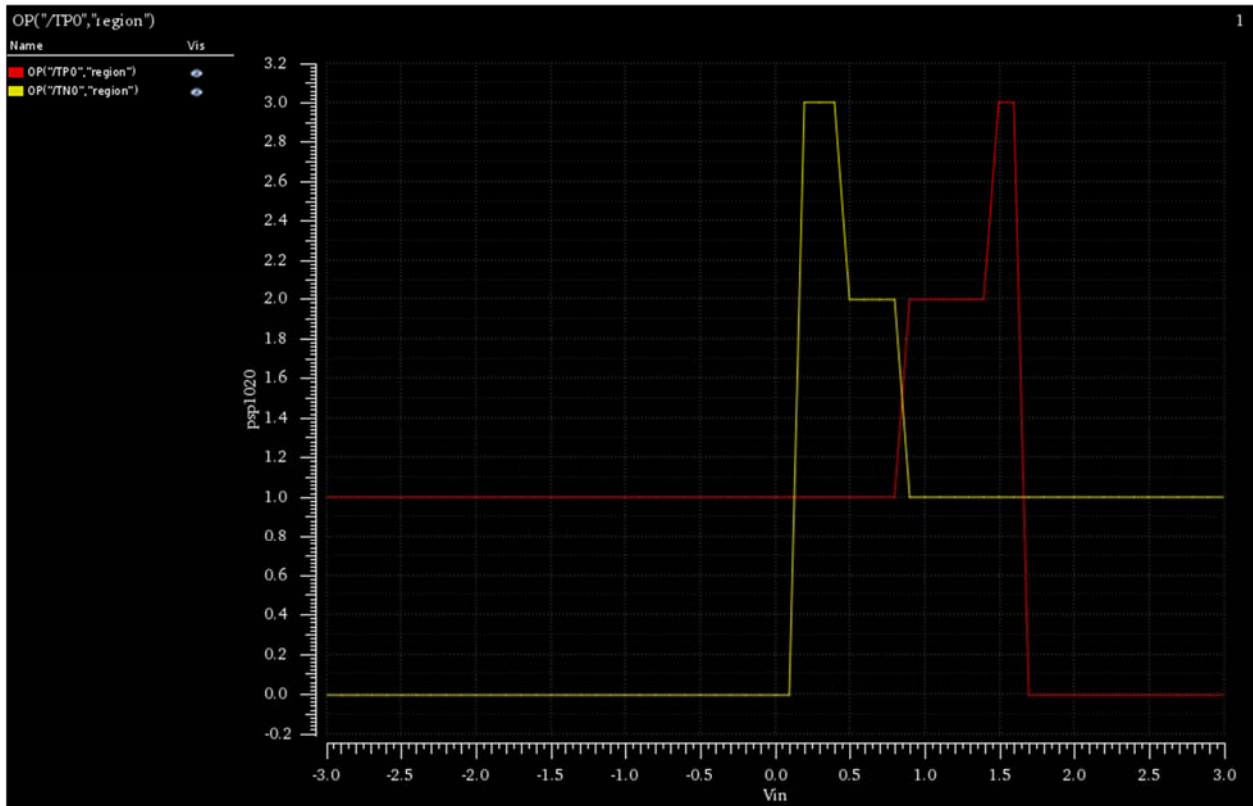


Figure 6-8: Region of Operation Plot for a Simple Inverter Circuit

Prelab

The prelab exercises are due at the beginning of the lab period. No late work is accepted.

1. Compare the two single-ended differential amplifiers discussed in this lab. Rate the differential gain, common mode gain, power supply voltage, CMRR and common mode input range. Include expressions for each design specification.
2. Design the simple differential amplifier in Figure 6-5 to obtain the following specifications:

Slew Rate	10 V/ μ s
Gain-Bandwidth Product	5 MHz
Common Mode Voltage Range	0.5 V
Power Supply	$V_{DD} = -V_{SS} = 0.9$ V
Load Capacitance	10 pF

3. Design the differential amplifier with cascode current mirrors in Figure 6-7 to obtain the following specifications:

Slew Rate	10 V/ μ s
Gain-Bandwidth Product	5 MHz
CMRR	> 60 dB
Power Supply	$V_{DD} = -V_{SS} = 0.9$ V
Load Capacitance	10 pF

Lab Report

1. Simulate the designs from the prelab, measure (include formulas used, do not derive them) and plot (use markers, remember the "m" hotkey):
 - a) Common mode range
 - b) Differential mode gain
 - c) Common mode gain
 - d) CMRR
 - e) GBW
 - f) Dominant pole p_1
 - g) Slew rate

Use any analysis necessary to obtain the most accurate measurements. Include these results in the lab report.

2. Layout the final designs. Repeat the above measurements. Be sure to include parasitic capacitance in the layout extraction. Include these results in you lab report as well as the LVS report (again NetID and time stamp required for credit).