ECEN 474/704 Lab 8: Two-Stage Miller Operational Amplifier

Objective

Design, simulate and test a two-stage operational amplifier

Introduction

Operational amplifiers (opamp) are essential components of analog system design. Integrated circuit design, as well as board level design, often uses operational amplifiers. This component is basically a high gain voltage amplifier used in many analog systems such as filters, regulators and function generators. This rudimentary device is also used to create buffers, logarithmic amplifiers and instrumentation amplifiers. Opamps can also function as simple comparators. Knowledge of operational amplifier functionality and design is important in analog design.

The symbol for an operational amplifier is shown in Figure 8-1. The basic device has two inputs and a single output. A fully differential version of the opamp has two outputs and is often used in high performance integrated circuit designs.
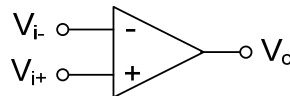

Figure 8-1: Operational Amplifier Symbol

The operational amplifier functions as a voltage amplifier. The relationship between the input and output voltage is given by:

$$V_o = A_{v0}(V_i^+ - V_i^-)$$

The amplifier has a high voltage gain ($A_{v0} > 1000$ for CMOS opamps). Due to the high gain, the linear region of an opamp is very narrow, so the opamp is commonly used in a negative feedback loop. Figure 8-2 illustrates the typical input-output characteristic tor an operational amplifier used with and without feedback. The open loop (without feedback) plot shows the linear region is only a few millivolts wide. From Figure 8-2, the open loop input-output characteristic is clearly nonlinear. Notice the closed loop linear region consists of almost the entire input voltage range. The application of feedback reduces the non-linearity, but also reduces the voltage gain.
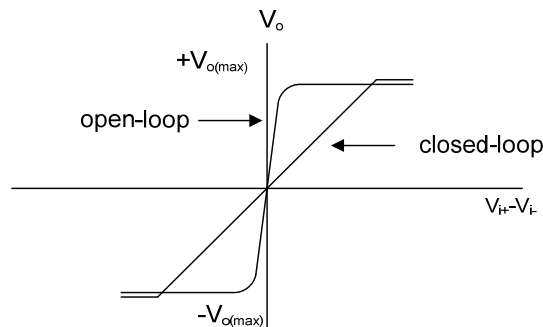

Figure 8-2: Input-Output Characteristic for an Opamp

The simplest operational amplifier is the simple differential amplifier studied earlier. This amplifier can be improved by adding a second stage as an inverting amplifier with a current source load. The two stage amplifier shown in Figure 8-3 is referred to as a Miller Opamp.
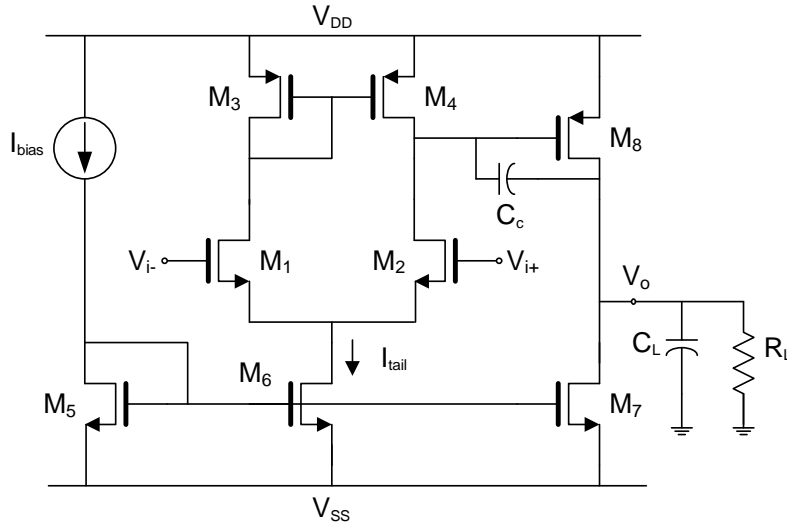
Figure 8-3: Two-Stage Miller Opamp

The Miller Opamp has a low frequency gain of:

$$A_{v0} = G_m(R_{out}||R_L)$$

The transconductance is given by:

$$G_m = \frac{g_{m1,2}}{g_{02} + g_{04}} g_{m8}$$

The output resistance is given by:

$$R_{out} = r_{07}||r_{08}$$

Design Description

The two-stage amplifier can be modeled as a cascade of two amplifiers, as illustrated in Figure 8-4. The first stage is a differential amplifier, which produces an amplified version of the difference in input signals. This stage determines the CMRR, slew rate and other performance specifications determined by the differential amplifier.
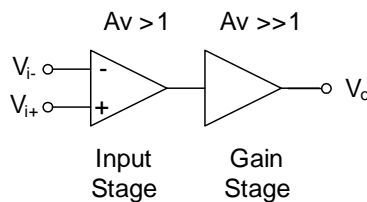

Figure 8-4: The Two Stage Operational Amplifier Model

The second stage is an inverting amplifier. The purpose of this stage is to provide a large voltage gain. The gain stage and the input stage create two poles, which affect the stability of the feedback system. Usually some form of compensation is required to assure the amplifier is stable at unity gain. Additional gain stages can be employed to increase the gain, but this degrades stability and requires complex compensation techniques.

The frequency response of an operational amplifier will be analyzed using the macro-model of the opamp shown in Figure 8-5. The capacitor C_{in} models the input capacitance of the opamp, which is mostly gate to source capacitance. The sub-circuit consisting of G_{mA}, R_A and C_A model the gain and frequency response of the input stage. The capacitance C_A includes the input capacitance of the second stage and the output capacitance of the first stage. The components G_{mB}, R_B and C_B model the second stage. The load capacitor and resistor are also included in R_B and C_B.
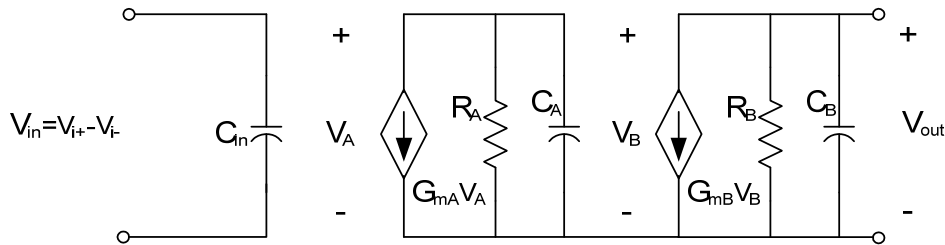

Figure 8-5: Operational Amplifier Macro-Model

The transfer function of the macro-model is given by:

$$H(s) = \frac{A_{v0}p_1 p_2}{(s+p_1)(s+p_2)} = \frac{\dfrac{G_{mA}G_{mB}}{C_A C_B}}{\left(s + \dfrac{1}{R_A C_A}\right)\left(s + \dfrac{1}{R_B C_B}\right)}$$

This transfer function assumes zero source resistance. Notice the two poles are approximately equal. The capacitors C_A and C_B are dominated by gate to source capacitances, and R_A and R_B are the parallel connected small-signal drain to source resistances. The pole-zero plot of this transfer function is illustrated in Figure 8-6.
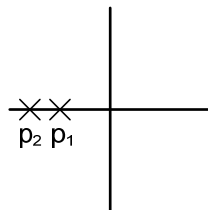

Figure 8-6: Pole-Zero Diagram for Uncompensated Opamp

Due to the poles being located close together and the large DC gain, the system in unlikely to be stable in unity-gain feedback configuration, therefore some form of compensation is required. The modified macro-model shown in Figure 8-7 uses capacitor C_C to compensate the frequency response of the opamp by splitting the two poles.
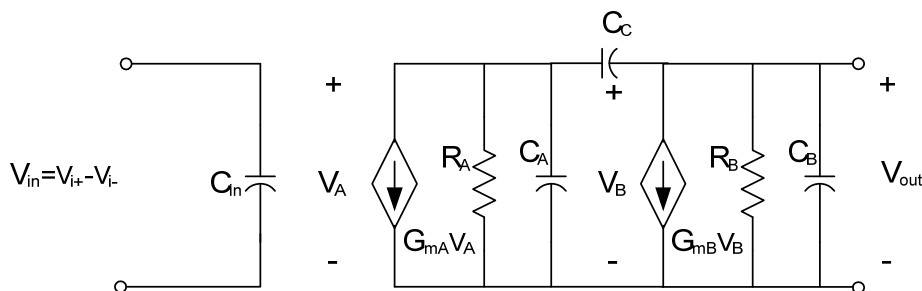

Figure 8-7: Operational Amplifier Macro-Model with Compensation Capacitor C_C

Assuming R_A is large ($R_A \approx R_B$ and $R_A \gg 1/G_{mB}$) and C_A is small ($C_B, C_C \gg C_A$), and using the results obtained from the inverting amplifier lab, the transfer function for the operational amplifier with the compensation capacitor is:

$$H_C(s) = \frac{\frac{A_{v0}p_1p_2}{z}(s-z)}{(s+p_1)(s+p_2)} = \frac{\frac{G_{mA}}{C_B}\left(s - \frac{G_{mB}}{C_C}\right)}{\left(s + \frac{1}{G_{mB}R_AR_BC_C}\right)\left(s + \frac{G_{mB}}{C_B}\right)}$$

These simplifying assumptions hold because capacitance C_B will include the capacitance of the load, and the compensation capacitance C_C can be chosen to be the size of the load capacitor. Also, for the two stage opamp, capacitance C_B will include the load capacitance C_L.

With the transfer function in factored form, we can find the open loop DC gain, poles and zero of the compensated opamp. They are given by:

$$A_{v0} = G_{mA}G_{mB}R_AR_B$$

$$p_1 = \frac{-1}{G_{mB}R_BC_CR_A} = \frac{-1}{|A_{v2}|C_CR_A}$$

$$p_2 = \frac{-G_{mB}}{C_B}$$

$$z = \frac{G_{mB}}{C_C}$$

$$GBW = \frac{G_{mA}}{C_C}$$

Note that the addition of the compensation capacitor C_C caused the poles to split. One pole moved closer to the origin by a factor of $A_{v2} = G_{mB}R_B$, while the other pole moved away from the origin by a factor of A_{v2}. This compensation technique is called "pole splitting". The pole-zero plot of this transfer function is illustrated in Figure 8-8. Also, notice the creation of a zero as a result of the transition path created by the capacitor.
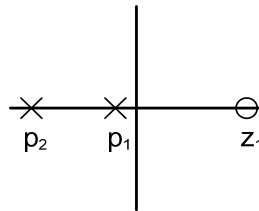

Figure 8-8: Pole-Zero Plot for a Compensated Opamp

Using the compensated opamp in a feedback loop produces the following transfer function:

$$A_C(s) = \frac{H_C(s)}{1 + H_C(s)\beta} = \frac{A_0(s-z)}{(s+p_1)(s+p_2) + A_0\beta(s-z)}$$

$$A_C(s) = \frac{A_0\left(s - \frac{G_{mB}}{C_C}\right)}{s^2 + \left(\frac{1}{G_{mB}R_AR_BC_C} + \frac{G_{mB}}{C_B} + \frac{G_{mA}}{C_B}\beta\right)s + \left(\frac{1}{R_AC_BR_BC_C} + \frac{G_{mA}G_{mB}}{C_BC_C}\beta\right)}$$

where:

$$A_0 = \frac{G_{mA}}{C_B}$$

The closed loop transfer function using the compensated amplifier can be approximated by:

$$A_C(s) = \frac{\frac{G_{mA}}{C_B}\left(s - \frac{G_{mB}}{C_C}\right)}{s^2 + \left(\frac{G_{mB}}{C_B} + \frac{G_{mA}}{C_B}\beta\right)s + \left(\frac{G_{mA}G_{mB}}{C_BC_C}\beta\right)}$$

The effect of the above simplification of the system is to assume the dominant pole is at the origin. Notice that when the system is in open loop ($\beta = 0$), the transfer function reduces to:

$$A_C(s) = \frac{\frac{G_{mA}}{C_B}\left(s - \frac{G_{mB}}{C_C}\right)}{s\left(s + \frac{G_{mB}}{C_B}\right)}$$

The factor β varies the position of the dominant pole from the origin to approximately the position of the non-dominant pole. Figure 8-9 illustrates the effect of feedback on the frequency response.
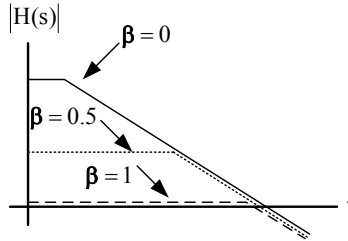

Figure 8-9: Open and Closed Loop Frequency Response

To assure the feedback system is stable at unity gain ($\beta = 1$), the phase margin must be examined. The phase margin is the amount of phase before phase inversion (180°) at the unity gain frequency. The expression for the phase margin is given by:

$$PM = 180° - \tan^{-1}\left(\frac{\omega_{0dB}}{p_1}\right) - \tan^{-1}\left(\frac{\omega_{0dB}}{p_2}\right) - \tan^{-1}\left(\frac{\omega_{0dB}}{z}\right)$$

$$PM = 180° - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right)$$

$$PM = 180° - \tan^{-1}(A_{v0}) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right)$$

$$PM \approx 90° - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right)$$

The phase margin is improved by moving the non-dominant pole and zero to higher frequencies away from the unity gain frequency. The phase margin can also be improved by using compensation techniques which place the zero in the left half plane.

The slew rate is determined by the compensation capacitance and the tail current:

$$SR = \frac{I_{tail}}{C_C}$$

The performance characteristics of the two-stage amplifier are summarized below:

$$A_{v0} = g_{m1,2}g_{m8}(r_{02}||r_{04})(r_{07}||r_{08}||R_L)$$

$$p_1 = \frac{-1}{g_{m8}(r_{07}||r_{08}||R_L)C_C(r_{02}||r_{04})} \qquad p_2 = \frac{-g_{m8}}{C_L} \qquad z = \frac{g_{m8}}{C_C}$$

$$GBW = \frac{g_{m1,2}}{C_C} \qquad SR = \frac{I_{tail}}{C_C}$$

$$PM \approx 90° - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right)$$

Monte Carlo Analysis

Monte Carlo analysis provides an accurate and powerful method for parametric yield estimation. The principle of Monte Carlo analysis can be defined as the generation of circuit figure of merit distributions as a function of statistically varying device model parameters that accurately reflect manufacturing process variations.

With Monte Carlo analysis, you can generate and save statistical information about a circuit's temperature and geometry dependent performance characteristics. The mathematics supporting Monte Carlo method proves that the probability distribution of the simulated results will be statistically the same as the actual measurements of a real circuit that has been fabricated.

Follow the steps below to run Monte Carlo simulations for A_{v0}, dominant pole, gain-bandwidth product and phase margin:

- **Schematic:** *Launch → ADE L*
- **ADE L:** *Setup AC Analysis*
- **ADE L:** *Tools → Calculator*
- **Calculator:** *Click on vf*
- **Schematic:** *Click on the output net*
- **Calculator:** *Select the expression, then click on function panel for each parameter:*
  - **A_v0:** *Click on "dB20", then click on "value" with "interpolate at"=0*
  - **Dominant Pole:** *Click on "bandwidth" with "Db"=3 and "Type"=low*
  - **Gain-Bandwidth Product:** *Click on "gainBwProd"*
  - **Phase Margin:** *Click on "phaseMargin"*
- **Calculator:** *Tools → Send Buffer to ADE Outputs (or click on* ⚙ *)*
- **ADE L:** *Outputs - Click on Save*

- **ADE L:** *Simulation → Netlist and Run (or click on ⏵)*
- **ADE L:** *Launch → ADE XL → Create New View   → OK → OK*
- **ADE XL:** *Run → Monte Carlo Sampling → Set options as shown in the figure below → OK*
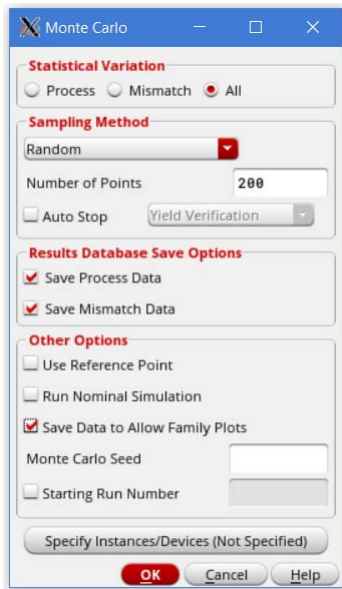
- **ADE XL:** *Wait until the analysis is complete (200 Passed/200 pts)*
- **ADE XL:** *Click on ⣿ → Histogram → Click on the expression → plot (see below)*
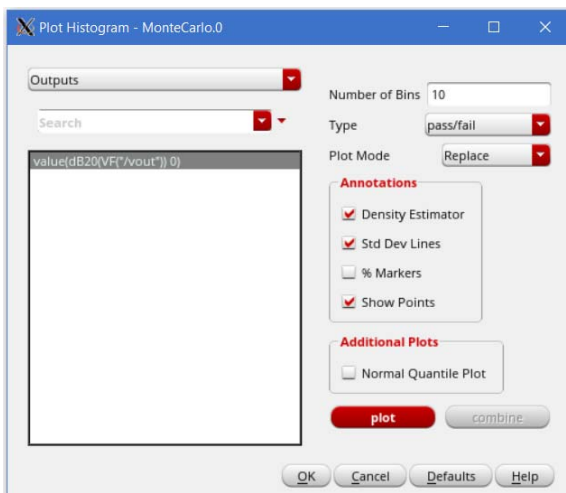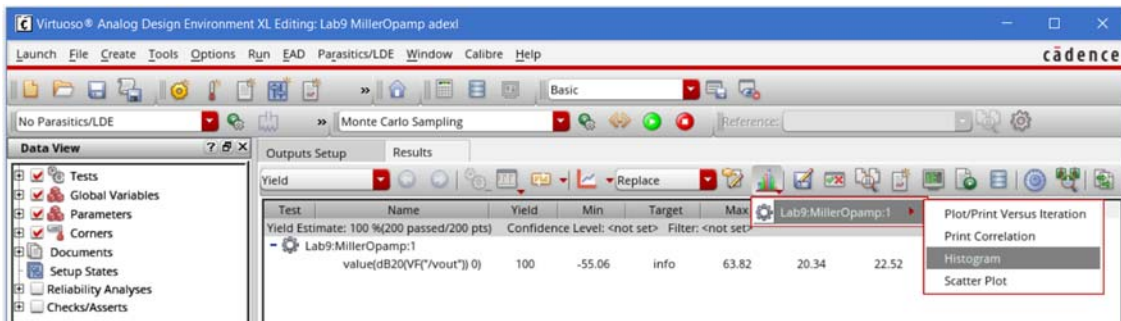
Plotting Power Supply Rejection Ratio (PSRR)

PSRR is a measure of the effect of power supply variation on the output voltage. To plot PSRR⁺, first determine A_{dm} in V/V. Next, set the AC inputs of the amplifier to zero, and insert an AC source (with magnitude 1) between V_{DD} and the amplifier. After running AC simulation, plot the following using the calculator:

$$PSRR = 20 \, log\left(\frac{A_{dm}}{vf\,(V_{out})}\right)$$

A plot of PSRR⁺ is shown in Figure 8-10, mark the lowest point for the worst case scenario. Repeat this process with the negative rail to obtain PSRR⁻.
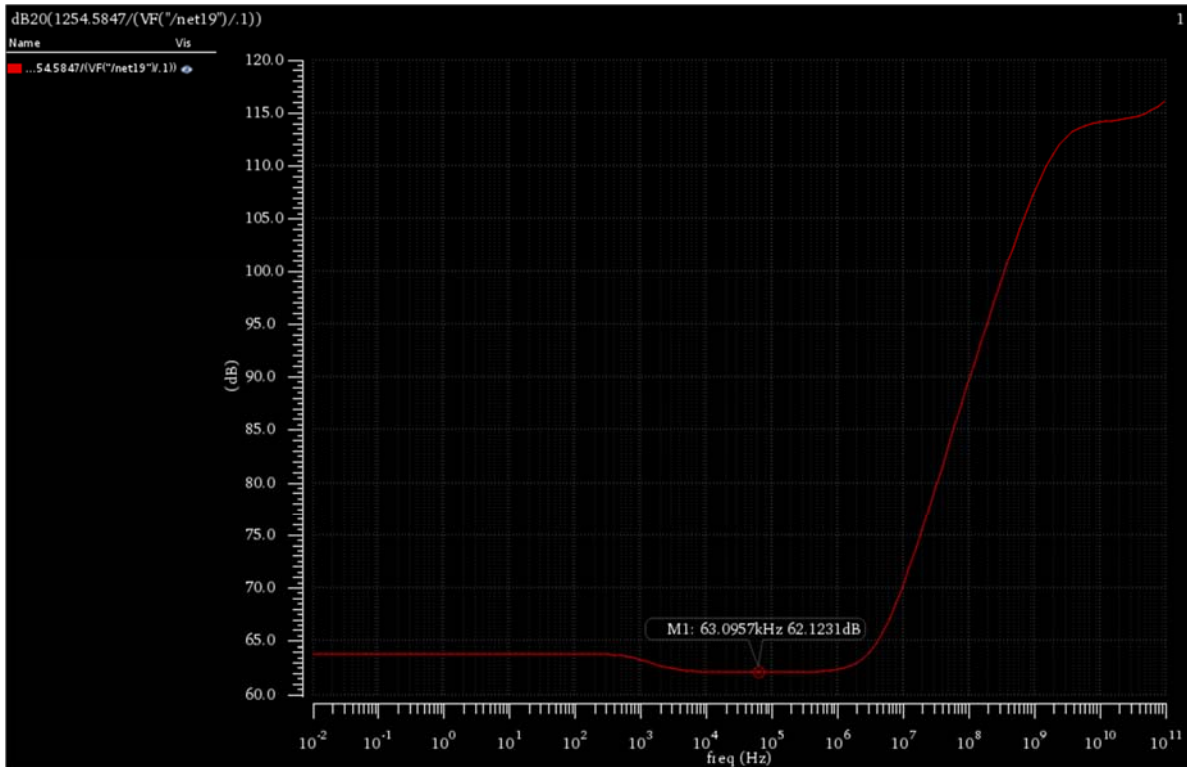

Figure 8-10: Plot of PSRR⁺

Prelab

The prelab exercises are due at the beginning of the lab period. No late work is accepted.

Design an operational amplifier of Figure 8-3 to obtain the following specifications:

A_{v0}	> 50 dB
CMRR	> 60 dB
GBW	> 2 MHz
PM	> 45°
Output Swing	> 1 V
Load Capacitance	30 pF
Power Dissipated	< 500 μW

Lab Report

1. Simulate the design from the prelab. Adjust the transistor sizes until all specifications are met. Provide plots of:

   - Frequency response
   - CMRR
   - PSRR$^+$
   - PSRR$^-$
   - Transient response

   On the appropriate plot above, mark the following measurements (remember the "m":hotkey for marker and the "a" and "b" hotkeys for measuring slope):

   - Slew rate
   - Phase margin
   - Gain-bandwidth product
   - Power Dissipation

2. Layout your final design using good layout techniques. Include the LVS report (with your NetID and time stamp). Plot and mark the simulations from part 1. Be sure to include parasitic capacitances in your extraction.

3. Run a Monte Carlo simulation on the opamp design. Be sure to run this simulation with process variation and mismatch. Generate histograms of the following parameters:

   a) Gain-bandwidth product
   b) Dominant pole
   c) Phase margin
   d) A_{v0}

   Comment on the impact of process variations and mismatch on each parameter.