March 29, 2018

ELEN-474/704: Analog VLSI

Course Projects

Preliminary report: Due on Apr. 17, 2018. **It must be submitted electronically**
Final report: May 1, 2018. **It must be submitted electronically**

Policies:

Project teams can consist of 1-3 students.

· Specifications and background. (5%)
· Search of existing solutions; use IEEExplore. (10%)
· Justify and define your architecture. (20%)
· Design and simulate your building blocks. (30%)
· Comparison of results (hand calculations and SPICE and/or spectre). (10%)
· Show the final results that proof your theory. (15%)
· Conclusions. (10%)

Pay attention to all sections!

After the project report exceeds 10 pages, usually the report size is inversely proportional to the quality of the results. Cover all the aforementioned issues, but please do not expend time discussing trivial or irrelevant stuff. In no more than 8 pages (you may have more pages due to the simulation results) you should be able to explain your work and be able to convince the instructor about the suitability of your approach. Please be clear and concise.

Here is a list of potential projects, but feel free to suggest topics.

Project #1. (High speed data converters)
Design a first-order switched-capacitor sample/hold and amplifier with closed-loop gain of 2 intended for pipeline ADCs. The sampling frequency will be 100 MHz, while the settling accuracy has to be better than 0.1%. The OTA must satisfy the following specifications: AV> 50dB, GBW>250 MHz (to be confirmed), open-loop phase margin> 45 degrees, in-band input referred noise level < 50 µV, and slew-rate > 250 V/µsec. Use supply voltages of +/- 0.9 Volts.

Project #2 (Audio-Video applications, high-resolution (Sigma-Delta Modulators) data converters, high-performance filters).
Design a first order switched-capacitor filter with a unity gain frequency of 4 MHz and dc-gain of 0 dB. Probe the stability and the precision of the integrator. Use a clock frequency of 40 MHz. The amplifier must satisfy the following specifications:
AV> 80 dB, GBW must be enough to achieve a settling error < 0.01% within the integrating period, open-loop phase margin> 48 degrees, input referred noise level < 50 µV, and output voltage swing > +/-0.4 V. Use supply voltages of +/- 0.9 Volts.

Project #3 (Extremely high-frequency applications, Wireless, Continuous-time filters).
Design a second order LP-BP OTA_C filter. The resonant/center frequency must be 100 MHz, quality factor of 10, pass-band gain = 0 dB. The basic integrator must also satisfy the following requirements: DC gain> 40 dB, excess phase at 100 MHz< 2 degrees, input referred noise level < 100 µV .The maximum input signal amplitude is 100 mV, and the THD<-50 dB. Use supply voltages of +/- 0.9 Volts.

Project #4 (Extremely high-frequency applications, Wireless, optical fiber, read channel, instrumentation).
Design a variable gain amplifier such that the voltage gain can be varied in more than one decade (1-10). The -3 dB bandwidth must be greater than 200 MHz, and linearity better than 1%; minimize both power consumption and silicon area. Use supply voltages of +/- 0.9 Volts.

Project #5 (Instrumentation).
Design an operational amplifier similar to the 741. AV≥106dB, GBW=1.2 MHz, slew-rate > 1µV/sec for a load capacitor of 10pF, output swing > +/- 0.4 volts. Use supply voltages of +/- 0.9 Volts; explore the possibility of using class AB output stage.

Project #6 (Optical fiber communications, transimpedance amplifiers).
Design a low-noise preamplifier for a photodiode that receives an ac current in the range of 0.1-5µA; photodiode's output impedance is modeled by a 0.25 pF capacitor. The frequency response must be larger than 1 GHz, and the trans-impedance gain = 60 dB; phase response should be linear; check your group delay. The output impedance of the preamplifier should be less than 200 ohms. Use supply voltages of +/- 0.9 Volts.

Project #7. (RF circuits)
Design a fast high gain multistage amplifier for data communication applications. Gain must be > 20dB, for an overall load capacitor of 1 pF; frequency bandwidth must be better than 1 GHz; compensate for differential DC offsets; low frequency corner must be smaller than 1 MHz. Minimize power consumption.

Your project suggestions are more than welcome! I encourage you to do a project that is not on this list, that YOU are interested in.