Texas A&M University
Department of Electrical and Computer Engineering

ECEN 474/704 – (Analog) VLSI Circuit Design

Fall 2016

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are 6 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		40
2		40
3		20
Total		**100**

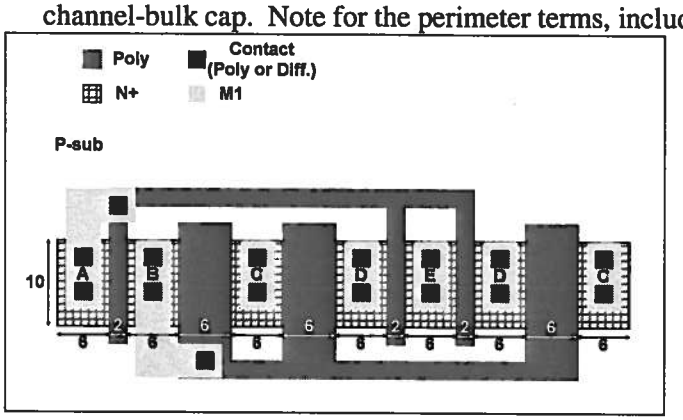
Name: SAM PALERMO

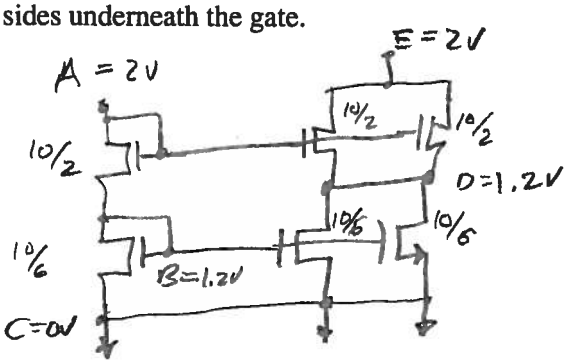
UIN: _____

Problem 1 (40 points)

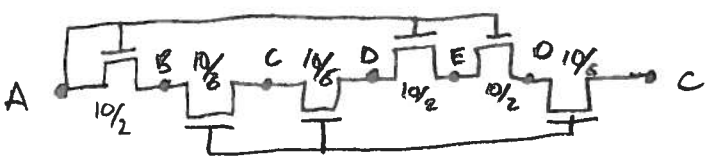
For the layout below, assume that all the commonly labeled diffusion areas are connected with the appropriate metal layers. Assume that V_A=2V, V_B=1.2V, V_C=0V, V_D=1.2V, V_E=2V, V_{T0}=0.7V, γ=0, and that all Spice parameters are given (i.e. C_j, C_{jsw}, C_{jc}, C_{ox}, C_{ov}). The dimensions are given in μm, with the poly gates having an L_D=0.1μm.

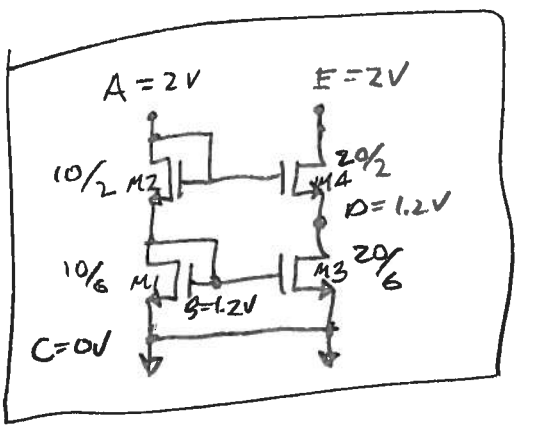
a) Draw the equivalent circuit. Combine all parallel transistors and given the total width and length of the equivalent transistors.
b) What region(s) are the transistors operating in?
c) **For node B only**, give an expression and calculate the total gate cap.
d) **For node D only**, give an expression and calculate the total junction cap, including the relevant channel-bulk cap. Note for the perimeter terms, include the sides underneath the gate.





a.





b. M1 $\Rightarrow V_{GS} = V_{DS} = 1.2V > V_T$

$V_{DS} > V_{GS} - V_T \Rightarrow$ Saturation

M3 same as M1

M2 $\Rightarrow V_{GS} = V_{DS} = 0.8V > V_T$

$V_{DS} > V_{GS} - V_T \Rightarrow$ Saturation

M4 same as M2

c. For $C_{GB} \Rightarrow$ M1 = Sat $\Rightarrow C_{gs} + C_{gd}$ (Shorted out)

$= \frac{2}{3}(10\mu)(5.8\mu)C_{ox} + 10\mu C_{ov}$

$= 38.7\mu^2 C_{ox} + 10\mu C_{ov}$

M3 = Sat $\Rightarrow C_{gs} + C_{gd}$

$= \frac{2}{3}(20\mu)(5.8\mu)C_{ox} + 20\mu C_{ov} + 20\mu C_{ov}$

$= 77.3\mu^2 C_{ox} + 40\mu C_{ov}$

Total $C_{GB} = 116\mu^2 C_{ox} + 50\mu C_{ov}$

d. $C_{j0} = A_D C_j + P_j C_{jsw} + L_{CBM4}$

$= (6\mu)(10\mu)(2)C_j + (6\mu+10\mu)(2)(2)C_{jsw}$

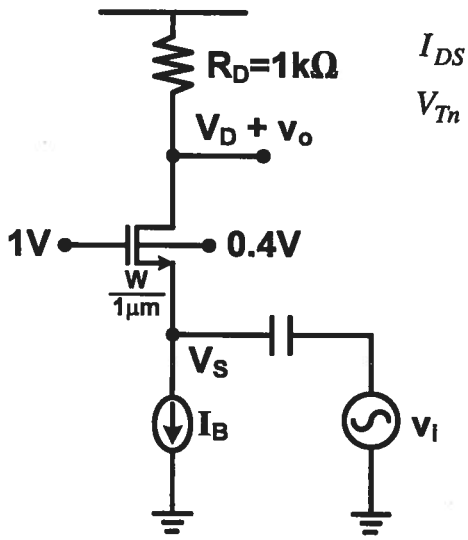
$+ \frac{2}{3}(20\mu)(1.8\mu)C_{jc}$

$C_{j0} = 120\mu^2 C_j + 64\mu C_{jsw} + 24\mu^2 C_{jc}$

Problem 2 (40 points)

For the circuit shown below, the transistor is operating in a fully velocity saturated region where its DC drain current is given exactly by the given equation.

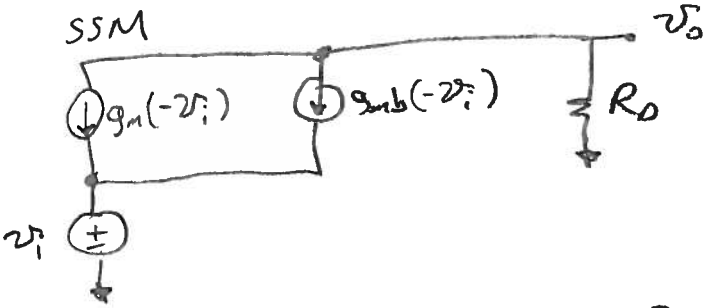
a. **Draw the low-frequency small-signal model of the circuit** (neglecting transistor capacitors) and **give an expression for the small-signal voltage gain of the circuit,** $A_v=v_o/v_i$, as a function of the relevant transistor conductances and the load resistor. Note, you can assume that the input AC–coupling capacitor acts as an ideal short.



Note N_o V_{DS} dependency $\Rightarrow g_o=0$, $r_o=\infty$

$$I_{DS}=v_{sat}C_{ox}W(V_{GS}-V_{Tn}) \Longrightarrow$$

$$V_{Tn}=V_{T0}+\gamma\left(\sqrt{|2\Phi_F|+V_{SB}}-\sqrt{|2\Phi_F|}\right)$$



$$v_o=-(g_m+g_{mb})(-v_i)R_D$$

$$A_V=\frac{v_o}{v_i}=(g_m+g_{mb})R_D$$

$$g_m=\frac{\partial I_D}{\partial V_{GS}}=V_{sat}C_{ox}W$$

$$g_{mb}=\frac{\partial I_D}{\partial V_{BS}}=V_{sat}C_{ox}W(-1)(-1)\frac{\gamma}{2\sqrt{|2\phi_F|+V_{SB}}}=\frac{\gamma g_m}{2\sqrt{|2\phi_F|+V_{SB}}}=\eta g_m$$

where $\eta=\frac{\gamma}{2\sqrt{|2\phi_F|+V_{SB}}}$

$A_v=v_o/v_i=(g_m+g_{mb})R_D$

b. Assume the following DC operating points for the drain and source voltages, $V_{S,Q}$=0.2V and $V_{D,Q}$=1V, and that $v_{sat}C_{ox}$=250μA/(V*μm), V_{T0}=0.7V, γ=0.45V$^{1/2}$, $2\Phi_F$=0.9V, and L_D=0.1μm. Calculate the necessary transistor width *W* for $|A_V|$=5V/V.

$$A_V=(g_m+g_{mb})R_D=(1+\eta)g_mR_D=(1+\eta)V_{sat}C_{ox}WR_D$$

$$W=\frac{A_V}{(1+\eta)V_{sat}C_{ox}R_D}=\frac{5}{(1.269)\left(250\frac{\mu A}{V\mu m}\right)1k\Omega}=15.8\mu m$$

W for $|A_V|$=5V/V = 15.8μm

$$\eta=\frac{0.45}{2\sqrt{0.9-0.2}}=0.269$$

Problem 3 (20 points)

a. Poly resistor design

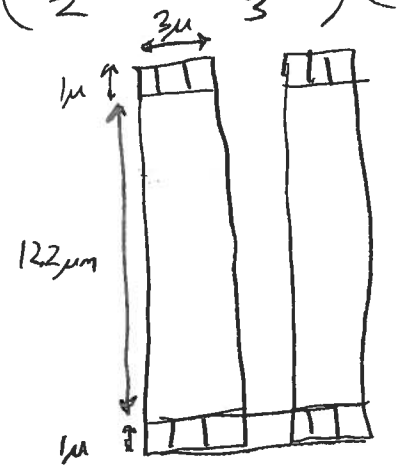
Design and sketch a layout of a 500Ω poly resistor. Assume that the poly R =60Ω/□, each (1µm x 1µm) contact has resistance of 10Ω, and fabrication tolerances limit the minimum unit resistor **width W** ≥ 3µm. Use at least 2 fingers in the resistor design. In the sketch clearly label the critical dimensions.

$$R_{total} = \left(\frac{2R_c}{n} + R_{\square}\frac{L}{W}\right)F$$ where n = # parallel contacts, F = # fingers (unit R)

$$L = \left(\frac{R_{total}}{F} - \frac{2R_c}{n}\right)\frac{W}{R_{\square}}$$

Set $W = 3\mu m$ $n = 3$ $F = 2$

$$L = \left(\frac{500}{2} - \frac{2(10)}{3}\right)\left(\frac{3\mu}{60}\right) = 12.2\mu m$$



b. Poly resistor parasitic capacitance

The poly resistor has a parallel-plate parasitic capacitance to substrate of 0.1fF/µm^2. What is the total parasitic capacitance of the resistor? Include the contact area in the capacitance calculation and assume that the capacitance is only due to the parallel-plate effect, i.e. neglect any fringing capacitance.

Resistor Area is $(12.2\mu m + 2\mu m)(3\mu m)(2) = 86.4\mu m^2$

$$C_{parasitic} = (86.4\mu m^2)(0.1fF/\mu m^2) = 8.64fF$$

c. N-well resistor design

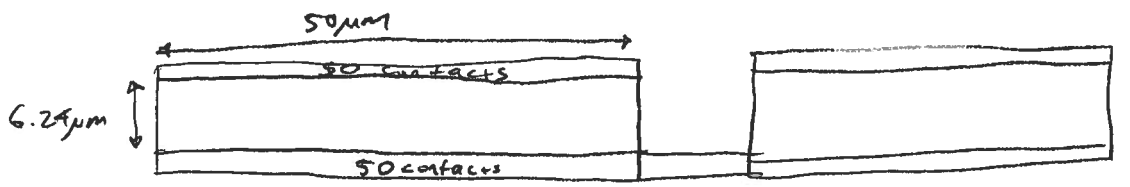
Design and sketch a layout of a 500Ω n-well resistor. Assume that the n-well R =2kΩ/□, each (1μm x 1μm) contact has resistance of 10Ω, and fabrication tolerances limit the minimum unit resistor **length L** ≥ 6μm. Use at least 2 fingers in the resistor design. In the sketch clearly label the critical dimensions.

$$R_{total} = \left(\frac{2R_c}{n} + R_{\square}\frac{L}{W}\right)F$$

$$L = \left(\frac{R_{total}}{F} - \frac{2R_c}{n}\right)\frac{W}{R_{\square}}$$

Set $F=2$, $W = 50\mu m$, $n = 50$

$$L = \left(\frac{500}{2} - \frac{2(10)}{50}\right)\left(\frac{50\mu m}{2k}\right) = 6.24\mu m$$



d. N-well resistor parasitic capacitance

The n-well resistor has a parallel-plate parasitic capacitance to substrate of 1fF/μm². What is the total parasitic capacitance of the resistor? Include the contact area in the capacitance calculation and assume that the capacitance is only due to the parallel-plate effect, i.e. neglect any fringing capacitance.

Resistor Area is $(6.24\mu m + 2\mu m)(50\mu m)(2) = 824\mu m^2$

$C_{parasitic} = (824\mu m^2)(1fF/\mu m^2) = 824fF$

e. If we have to use the 500Ω resistor for a high-frequency application, which design should we choose, the poly or n-well design? Why?

Poly R ⇒ Less Capacitance

Scratch Paper