Question 1. 35 points
The folded-cascade amplifier shown below uses two complementary differential pairs to increase the overall transconductance.

a) Give an expression for the DC current flowing through M3 and M4.

\[ I_{M3} = I_{M4} = \frac{2}{3} I_{TAIL} \]

\[ G_m = g_{mN} + g_{mP} \]

\[ A_v = G_m R_{out} \]

\[ R_{out} \approx \frac{r_o (g_{m3} (r_{o2} // r_{o1}))}{r_{o1} (g_{mp} (r_{os} // r_{on}))} \]

- 3 poles at output node and 2 cascode nodes

\[ W_{p1} = -\frac{1}{R_{out}C_w} = -\frac{1}{R_{out} (C_{b3} + C_{gd3} + C_{b4} + C_{gd4})} \]

\[ W_{p2} = -\frac{g_{m4}}{C_{cascade}} = -\frac{g_{m4}}{(C_{db4} + C_{gd4} + C_{gs4} + C_{b5} + C_{gd5})} \]

\[ W_{p3} = -\frac{g_{m3}}{C_{cascade}} = -\frac{g_{m3}}{(C_{db3} + C_{gd3} + C_{gs3} + C_{b2} + C_{gd2} + C_{gs2} + C_{sb3})} \]

- 2 zeros from N-MOS inputs \( C_{gd} \)

\[ W_{z1} = +\frac{g_{min}}{C_{gdN}} \]

\[ W_{z2} = +\frac{g_{mip}}{C_{gdP}} \]
A simplified version (bias circuitry is not shown) of a two-stage amplifier without phase compensation is shown in the figure below. The capacitors and resistors are due to the parasitic capacitors and output resistance of the transistors. Give a design procedure and fundamental equations for finding the bias currents, transistor dimensions and the miller capacitor required to satisfy the following constraints:

1. Slew-rate > 10 V/usec
2. Phase margin > 45 degrees.
3. Noise density < 10 nV/Hz
4. GBW > 10 MHz
5. DC gain > 80 dB

Explain your answers; and do not try to find numerical values. Just give a design procedure, and be sure you are covering all aspects of the design.

Most critical specs are $\Phi_{\text{margin}}$ and DC gain

In order to have $\Phi_{\text{margin}} > 45^\circ$: $\omega_p > \omega_u = Av_0\omega_p = 10^4\omega_p$

w/o any compensation poles are only spaced by a factor of $\sqrt{2}$

$\Rightarrow$ Miller Compensation is necessary

w/Miller cap, GM: $\omega_p = \frac{g_{m2}}{C_2} = \frac{g_{m2}}{5pF} \geq \frac{2\pi}{10\text{MHz}}$

$\Rightarrow g_{m2} \geq \pi \times 10^{-4} \text{ A/V}$

DC gain = $g_{m1} (1\text{M}) g_{m2} (1\text{M}) > 10^4$

$g_{m1} > \frac{10^4}{(10^{-12}\text{ A}) (1\times 10^{-4}\text{ A/V})} = 31.8 \text{ m}^2/\text{V}$

The noise spec will also set $g_{m1}$

\[
V_{n,jin}^2 = \frac{i_{n,inp}^2}{g_{m}} = \frac{8}{3} KT \left[ \frac{g_{m2} + \frac{g_{m1} g_{m2}^2 (1\text{M})^2}{g_{m1}^2 g_{m2}^2 (1\text{M})^4}}{g_{m1} g_{m2} (1\text{M})^2} \right] \left( \frac{V^2}{Hz} \right)
\]
\[ V_{n, in} = \frac{8}{3} kT \left( \frac{1}{g_{m1}} \right) \left[ 1 + \frac{1}{g_{m1} \cdot g_{m2} \cdot (10^{-2})^2} \right] \left( \frac{V_{ref}}{Hz} \right) \]

\[ V_{n, in} = \sqrt{V_{n, in}^2} \left( \frac{V}{Hz} \right) \]

⇒ We can approximate this by

\[ V_{n, in}^2 = \frac{8kT}{3g_{m1}} < (10^{-8})^2 \frac{V^2}{Hz} \]

\[ g_{m1} > \frac{8 \cdot (4.14 \times 10^{-21})}{3 \cdot (10^{-16})} = 110 \mu A/V \]

⇒ Noise spec sets \( g_{m1} !!! \) (Greater than DC gain spec)

\[ GBW = \frac{g_{m1}}{CM} > 2\pi \left( 10 \text{MHz} \right) \]

\[ CM < \frac{g_{m1}}{2\pi \left( 10 \text{MHz} \right)} = \frac{110 \mu A/V}{2\pi \left( 10 \text{MHz} \right)} = 1.75 \text{ pF} \]

⇒ Slew rate can be set by either 1st or 2nd stage.

\[ SR = \min \left[ \frac{I_1}{CM + 2\text{pF}}, \frac{I_2}{5\text{pF}} \right] = 10 \text{V/\mu s} \]

Note: The RHP zero = \( + \frac{g_{m2}}{CM} = \frac{11 \times 10^{-4}}{5.75 \text{pF}} = 2\pi \left( 28.6 \text{MHz} \right) \)

will degrade the \( \phi_{margins} \). May need to increase \( g_{m2} \) or add a series \( R \) in compensation.
Question 3. 30 points

Sketch the common-mode feedback circuit for the following fully-differential amplifier such that the DC level of the outputs is zero volts. Do not attach resistors to the OTA outputs, and do not use ideal buffers. Explain the role of each building block used and discuss the stability issues; phase margin of the common-mode feedback > 45 degrees.

Assume that the bias current flowing through each PMOS device is fixed at IB.

Equivalent Amp for CMFB

\[
\text{Loop Gain} G_{\text{loops}} = \left( \frac{g_{m1}}{g_{m2}} \right) \left( -g_{m3} \right) \left( \frac{C_4}{2 (2g_{m4}r_{03})} \right) \left( \frac{r_{05}}{2} \right)
\]

\[
= \frac{g_{m1}}{g_{m2}} \left( -\frac{g_{m3} r_{05}}{2} \right)
\]

Poles at

\[
\frac{1}{r_{05}C_1}, \quad \frac{2g_{m1}}{C_2}, \quad \frac{g_{m2}}{C_3}, \quad \frac{2g_{m4}}{C_4}
\]

Dominant pole probably wp2

Assuming the other 2 poles are sufficiently high

wp2 \(>\) GBW for \( \phi_{\text{margin}} > 45^\circ \)

\[
C_{\text{BW}} = \frac{1}{\text{wp1}} = \frac{g_{m1}}{g_{m2}} \left( \frac{g_{m3} r_{05}}{2} \right) \left( \frac{1}{r_{05}C_1} \right) = \frac{g_{m1} g_{m3}}{2g_{m2} C_1}
\]

\[
\frac{g_{m2}}{r_0} > \frac{g_{m1} g_{m3}}{2g_{m2} C_1}
\]
For the following bandgap circuit, consider that \( n = 2 \) (you may think that are 2 BJTs is parallel). Give the 3 fundamental equations that define its operation.

\[
\begin{align*}
A_{E2} &= 2 A_{E1} \\
V_{i_{ref}} &= V_{EB1} + V_{R1} \\
V_{R3} &= V_{EB1} - V_{EB2} = \Delta V_{EB} \\
V_{R2} &= \frac{R_2}{R_3} \Delta V_{EB} = K \Delta V_{EB} \\
V_{i_{ref}} &= V_{EB1} + V_{R2} = V_{EB1} + \frac{R_2}{R_3} \Delta V_{EB} \\
\Delta V_{EB} &= V_{EB1} - V_{EB2} = \frac{KT}{q} \ln \left( \frac{J_1}{J_2} \right) \\
\frac{J_1}{J_2} &= \left( \frac{I_1}{A_{E1}} \right) \left( \frac{2A_{E1}}{I_2} \right) = \frac{2I_1}{I_2} = 2 \frac{V_{i_{ref}} - V_{EB1}}{V_{i_{ref}} - V_{EB1}} = \frac{2R_2}{R_1} \\
V_{i_{ref}} &= \frac{KT}{q} \ln \left( \frac{2R_2}{R_1} \right) + \frac{R_2}{R_3} \Delta V_{EB} \\
\Rightarrow R_1 \text{ and } R_2 \text{ set by } I_1, I_2, V_{i_{ref}}, V_{EB01} \\
\Rightarrow R_3 \text{ set by } K = \frac{1.26V - V_{EB01}}{\frac{KT}{q} \ln \left( \frac{J_1}{J_2} \right)}
\end{align*}
\]