January 31, 2018

ECEN 474/704

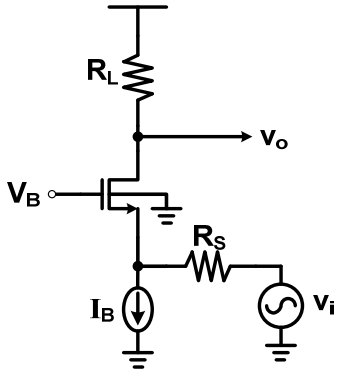
Homework #1

Due: 2-8-2018, 5:00PM

Homeworks will not be received after due.

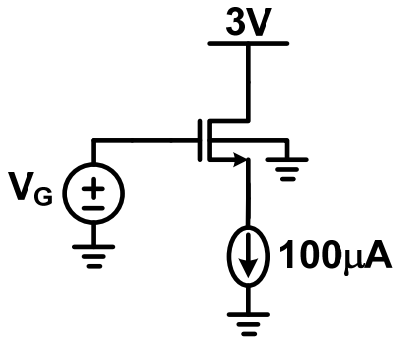
Instructor: Sam Palermo

1. **(40 points)** MOSFET Small-Signal Analysis
   a) Draw the small-signal model for the MOSFET amplifier circuit below, including the necessary capacitors. For the MOSFET, assume saturation, infinite output impedance, and consider relevant device capacitors. Also, include the body transconductance effect, g_{mb}. **(10 points)**
   b) Derive the small-signal transfer function, $v_o(s)/v_i(s)$. This should be given as a function of g_m, g_{mb}, C_{gs}, C_{gd}, C_{sb}, C_{db}, R_S, and R_L. **(20 points)**
   c) Give expressions for the DC gain and the amplifier's poles and zeros (if any). **(10 points)**



2. **(10 points)** Body Effect on Threshold Voltage

For the circuit below, what is the value of V_G that causes the V_T of the transistor to increase to 0.8V? Assume the transistor is in saturation and that V_{T0}=0.7V, γ=0.45V$^{1/2}$, $2\Phi_F$=0.9V, μC_{ox}=130μA/V^2, (W/L)=(10μ/0.6μ).



3. **(30 points)** Layout & Transistor Capacitors

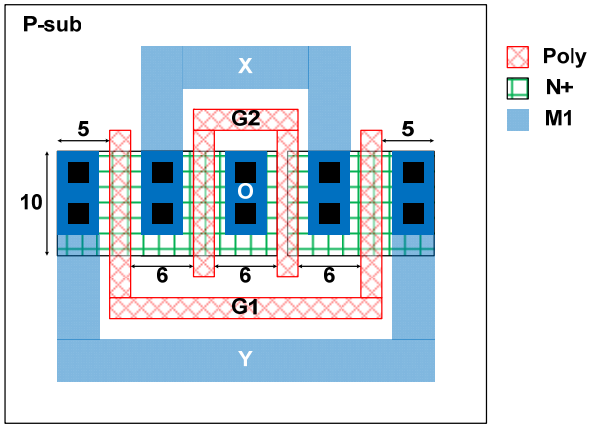
For the following layout, assume that all Spice parameters are given (i.e. C_{js}, C_{jsw}, C_{ox}, C_{ov}). The dimensions are given in λ units, where λ=0.5µm. Assume that all poly gates have L=1µm and L_D=0.05µm.

a) Draw the equivalent circuit. **Combine all parallel transistors. (15 points)**

b) Assume that V_O=0.5V, V_X=0.4V, V_Y=0V, V_{G1}=1V, V_{G2}=1.5V. Also assume that the p-substrate is grounded, V_{T0}=0.7V, and γ=0. What region are the transistors operating in? **(5 points)**

c) Give an expression for the total gate capacitance of the transistors. **(5 points)**

d) Give an expression for the total junction capacitance at nodes O, X, and Y. Note for the perimeter terms, include the sides underneath the gate. **(5 points)**



4. **(20 points)** Capacitor Matching

a) Sketch a layout that matches two capacitors of unit size 8 and 3.75. The key is to match the perimeter-to-area ratio - see the lab manual or the Razavi text for reference. Assume that the unit capacitors are sized 4µm x 4µm. Make sure to give the non-unit capacitor dimensions. **(15 points)**

b) Assume that the process accuracy is 0.1µm, i.e. round all dimensions to the nearest 0.1µm. What is the percent error? **(5 points)**

$$\textbf{Percent Error} = \frac{\textbf{Actual Ratio - Ideal Ratio}}{\textbf{Ideal Ratio}} \times 100\%$$