Feb 20, 2018

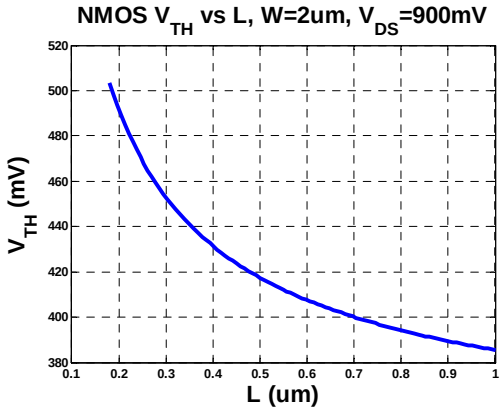
ECEN 474

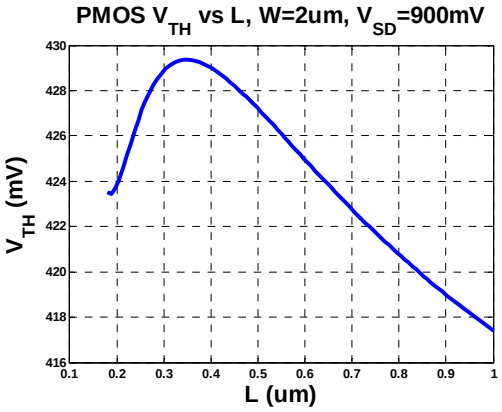
Homework #2 Solution

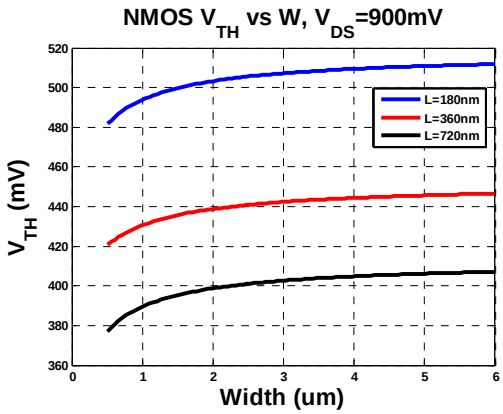
1. **(50 points)** Technology Characterization for Design

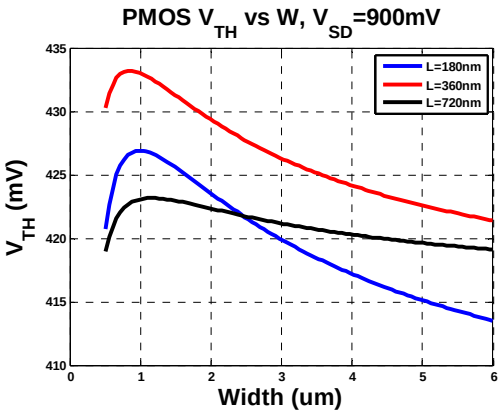
In this problem, we will extract some of the key MOSFET parameters used in circuit design. For all the following, extract the required data and plots for both the NMOS AND the PMOS device. For the PMOS device swap the polarity of the given bias conditions, i.e use V_{SD} for V_{DS} and V_{SG} for V_{GS}.

a) Threshold Voltage Dependency on Width & Length.

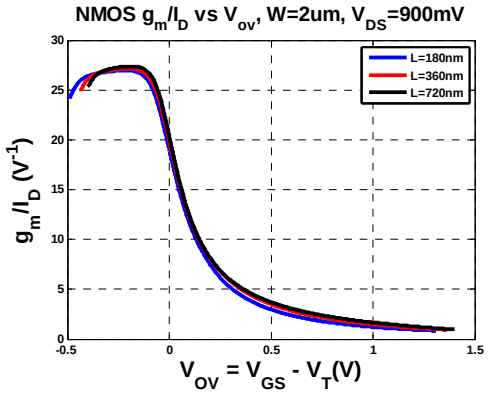


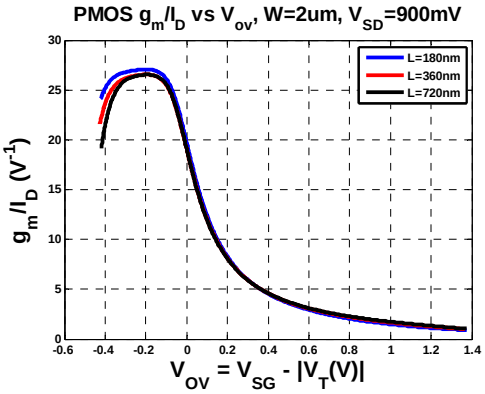


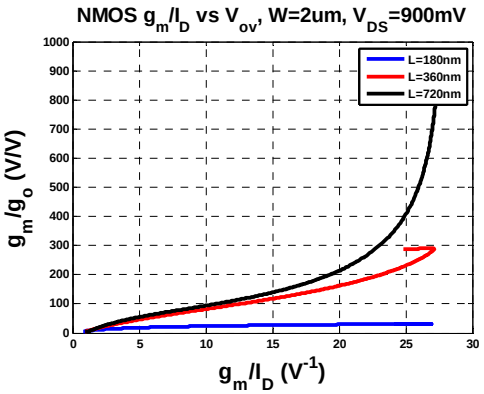


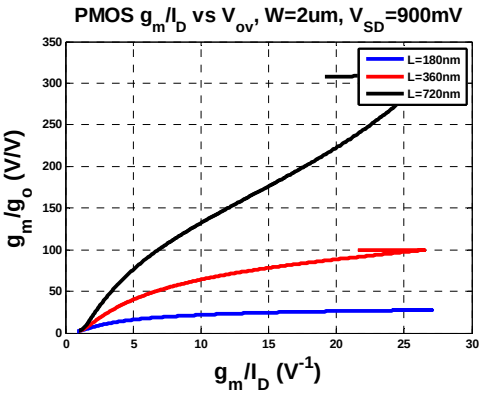


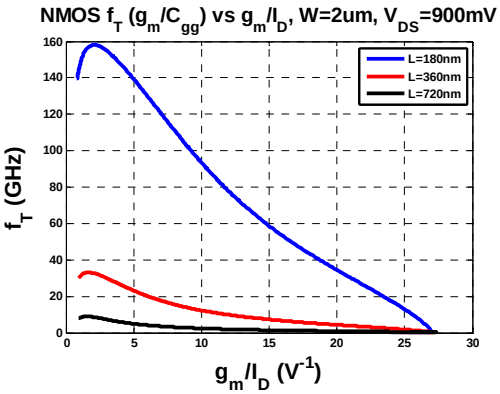
c) Essential Design Plots. Note, I inverted the PMOS current to more easily compare the NMOS and PMOS data.

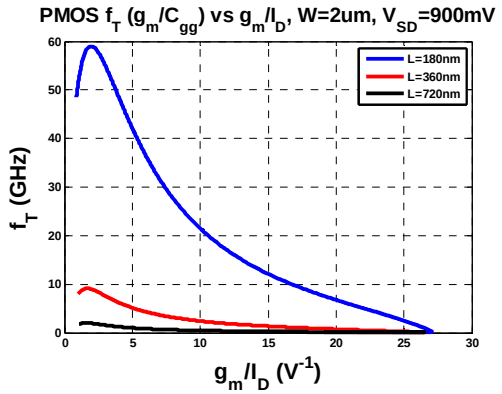


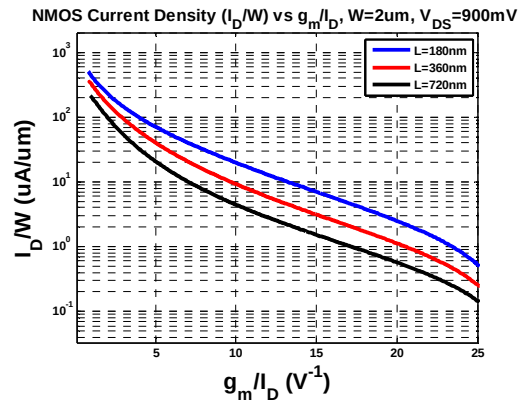


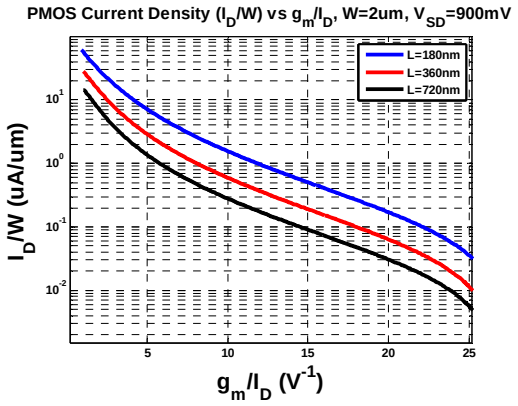






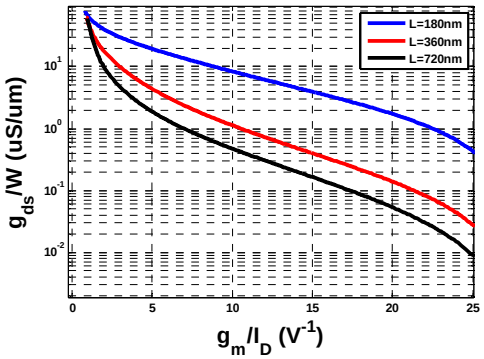




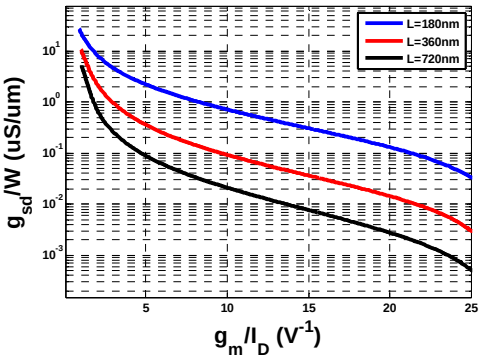


d) Other Useful Design Plots

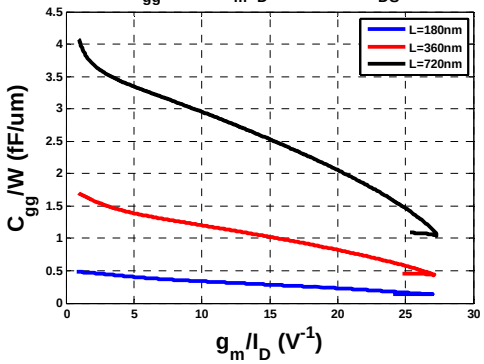
NMOS g_{ds}/W (uS/um) vs g_m/I_D, W=2um, V_{DS}=900mV



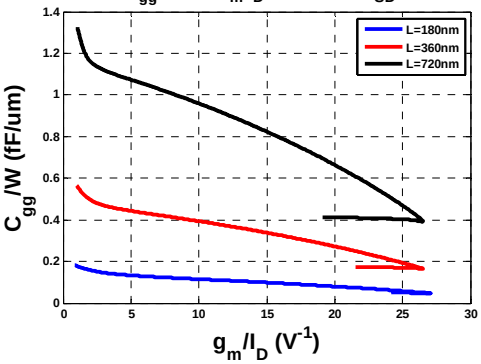
PMOS g_{sd}/W (uS/um) vs g_m/I_D, W=2um, V_{SD}=900mV



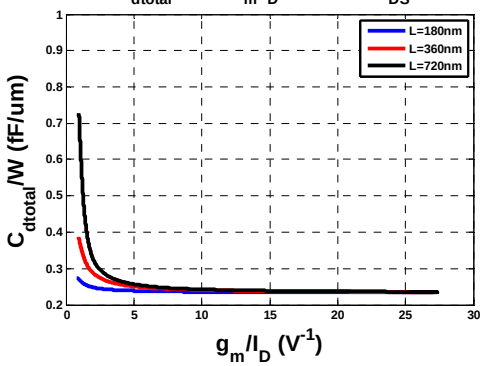
NMOS C_{gg}/W vs g_m/I_D, W=2um, V_{DS}=900mV



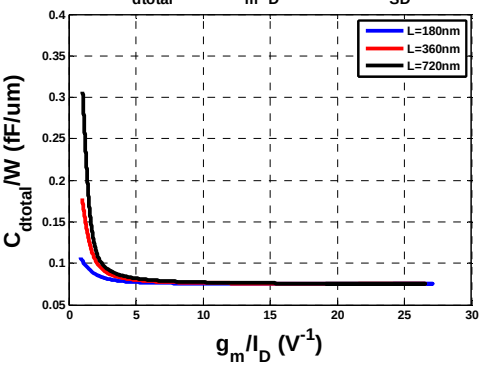
PMOS C_{gg}/W vs g_m/I_D, W=2um, V_{SD}=900mV



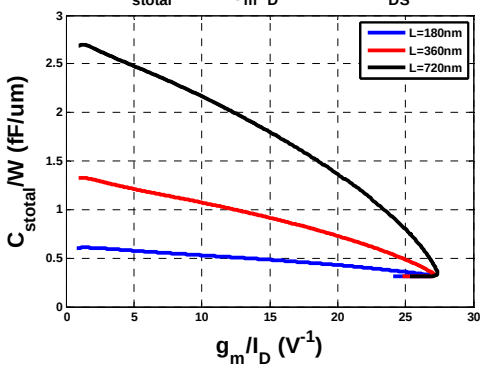
NMOS C_{dtotal}/W vs g_m/I_D, W=2um, V_{DS}=900mV



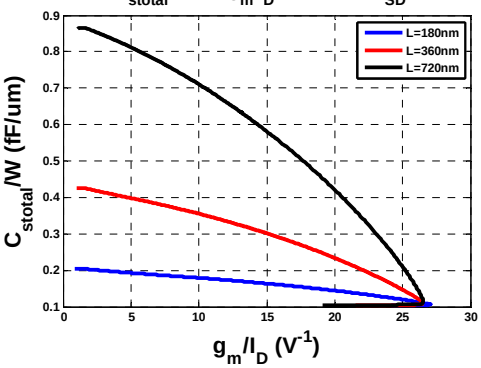
PMOS C_{dtotal}/W vs g_m/I_D, W=2um, V_{SD}=900mV



NMOS C_{stotal}/W vs g_m/I_D, W=2um, V_{DS}=900mV



PMOS C_{stotal}/W vs g_m/I_D, W=2um, V_{SD}=900mV



Problem 2 Final Design

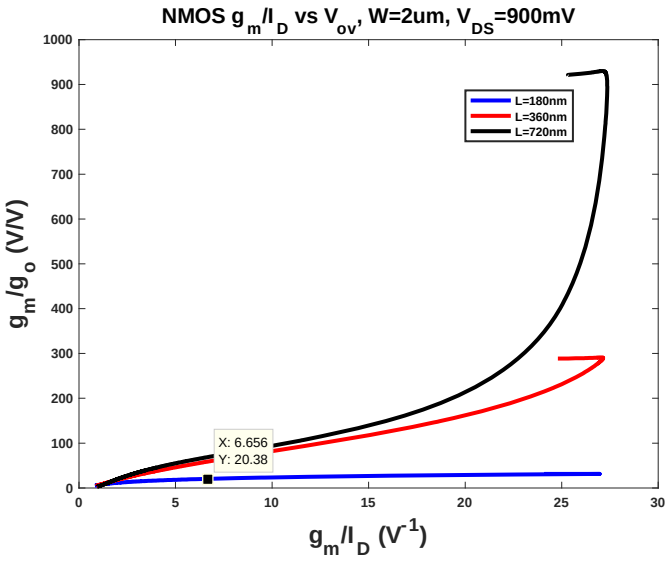
$$g_m = \omega_u C_L = 2\pi(200M)(5pF) = 6.3mA/V$$

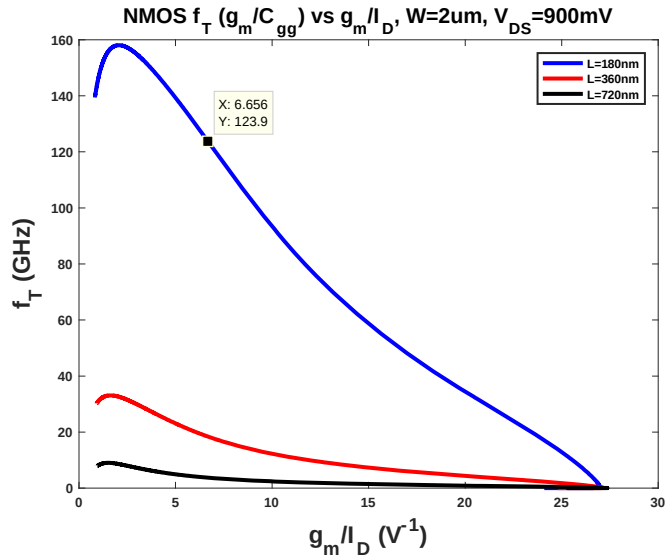
$$R_L = \frac{Av}{gm} = \frac{5\times 20\%margin}{6.3mA/V} = 950\Omega$$

For output common-mode level, $1.8V - I_D R_L = 0.9V \rightarrow I_D = 947.4uA$

Therefore, gm / I_D =<u>$6.65V^{-1}$</u>

From this spec, relatively low gm/I_D yields an operation in <u>strong-inversion region.</u> Due to the relaxed dc gain, minimum channel length, L=180nm is used.

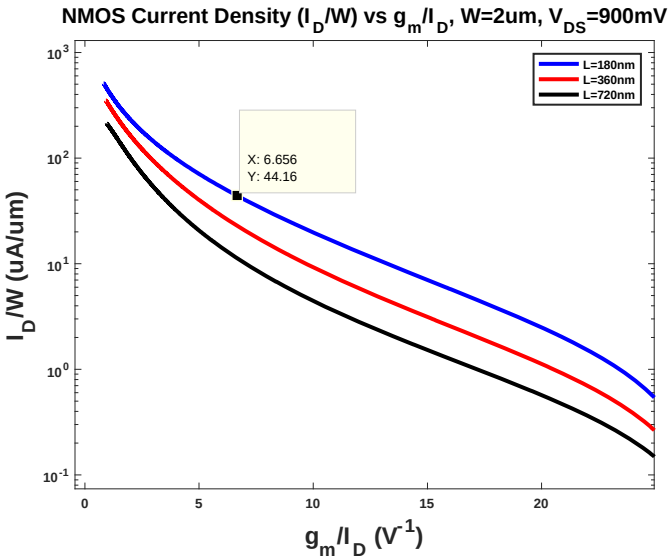




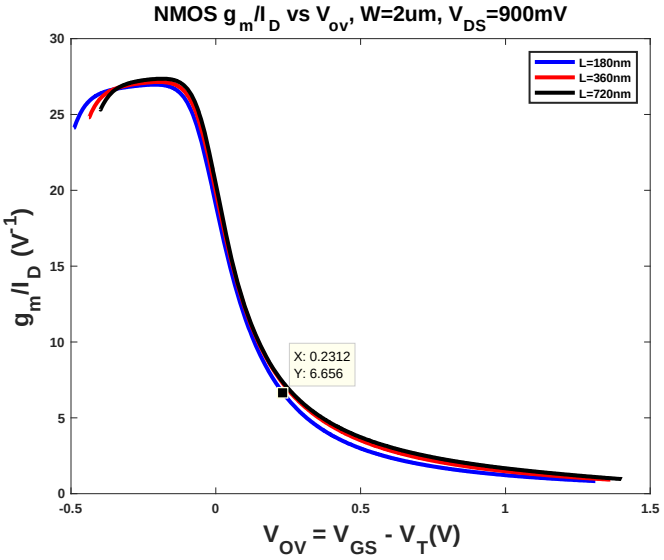
In the strong inversion, low gm/I_D is desirable for sufficiently high bandwidth.

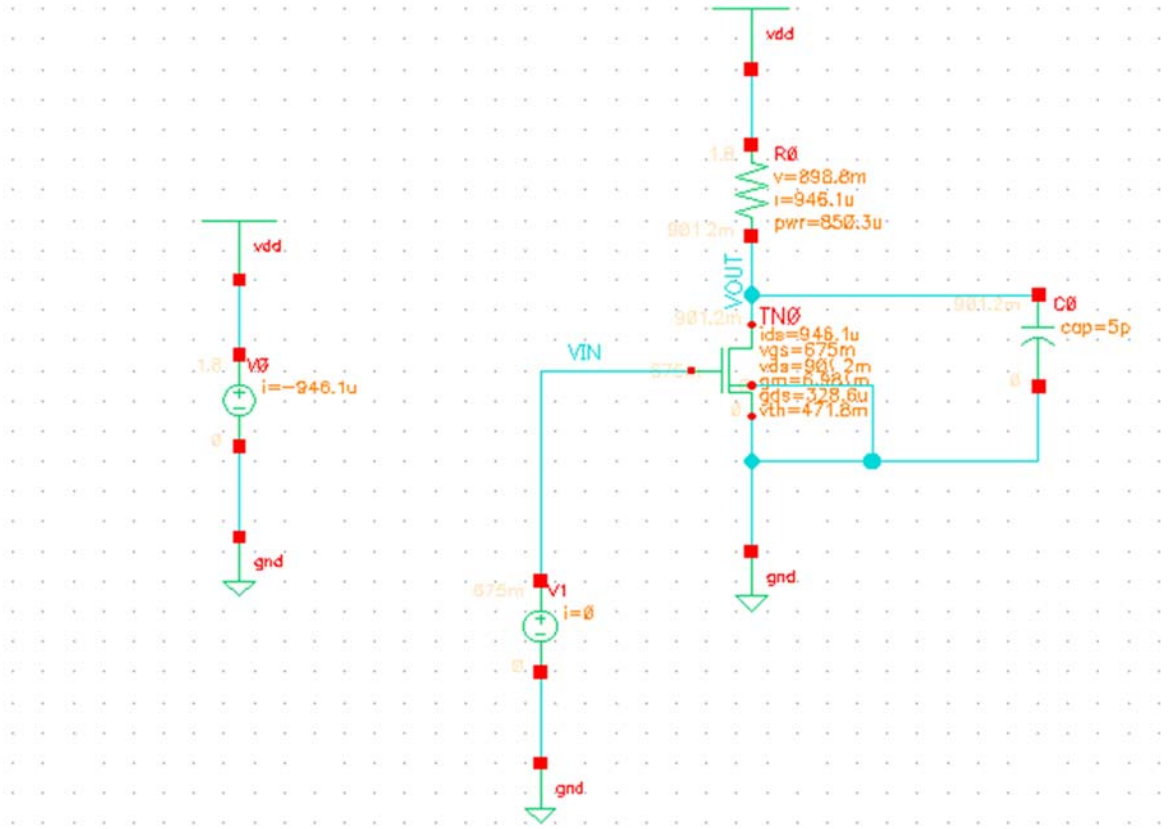
Current Density is 44.16 uA/um for gm/I_D = 6.65V^{-1}. Therefore,$W = \frac{I_D}{I_D/W} = \frac{947.4uA}{44.16uA/um} = 21.45um$

NMOS with **<u>2um x 12 fingers</u>** is used.

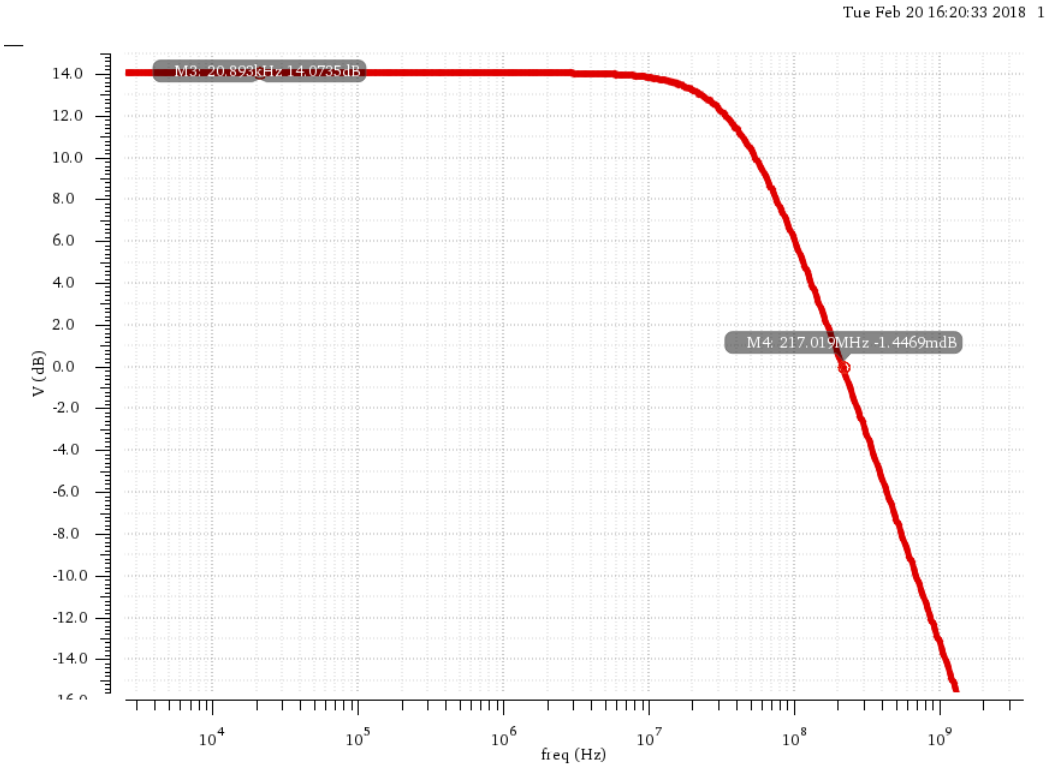


And for gate biasing 675mV is chosen from the Current Density vs. Vgs curve.





With minor adjustment in the gate-bias voltage **Av=14.07dB(>5 V/V) and the GBW = 217MHz (>200MHz)**.



beff	45.82m	ctype	1	region	2
cbb	3.155f	fknee	2.226M	rg	NaN
cbd	70.59a	fug	44.78G	rout	3.044K
cbg	1.486f	gds	328.6u	sdi	0
cbs	1.599f	gjd	30.38f	sdint	1
cdb	555.5a	gjs	2.034f	sfl	0
cdd	29a	gm	6.981m	siavl	0
cdg	2.705f	gmb	1.385m	sid	97.97y
cds	-3.231f	iavl	3.016p	sig	1.269e-39
cgb	1.635f	ibe	-3.026p	sigd	0
cgbol	0	idb	3.026p	sigs	0
cgd	-109a	ide	946.1u	sqrtsff	0
cgdol	7.659f	ids	946.1u	sqrtsfw	0
cgg	8.828f	igb	0	ssi	0
cgs	7.302f	igcd	0	u	21.25
cgsol	8.328f	igcs	0	vbs	286.5p
cigid	403m	igd	0	vds	901.2m
cjd	5.649f	ige	0	vdss	210.6m
cjdbot	9.173e-27	igidl	995.5e-81	vearly	2.879
cjdgat	5.649f	igisl	0	vgs	675m
cjdsti	-0	igs	0	vgt	203.2m
cjs	7.609f	ijd	-9.996f	vsat	690.6m
cjsbot	12.2e-27	ijdbot	-1.327z	vsb	-286.5p
cjsgat	7.609f	ijdgat	-9.996f	vth	471.8m
cjssti	-0	ijdsti	0	vto	493.9m
csb	964.5a	ijs	582.8e-27	vts	493.9m
csd	67.42a	ijsbot	14.7e-30		
csg	4.637f	ijsgat	582.8e-27		
css	5.669f	ijssti	0		
		isb	-582.8e-27		
		ise	-946.1u		
		lpoly	180n		

With the V_{GS} adjustment, the hightlighted dc operating point parameters are close to design chart generated from BSIM-4 transistor simulation data.