Due: October 31, 2012, 5:00 P.M.  
**Homeworks will not be received after due.**
Instructor: Sam Palermo

The following schematic corresponds to a single-ended amplifier already discussed in class; attach a load capacitor CL=1 pF. Design your current source to get a low-frequency common-mode gain (voc/vic) < -40 dB. Use power supplies of VDD=1.5V and VSS=-1.5V. Also, implement the tail current source at the transistor-level.

a) Design the circuit (find transistors dimensions and bias current for the differential pair) for a differential gain greater or equal than 20 dB (vo/vid) and a transconductance gain of 1 mA/V.

b) Simulate your circuit and find its AC response in the range 10^-10^6 Hz
   a. Transconductance gain (magnitude and phase response)
   b. Common-mode gain (magnitude and phase response)

c) Simulate your circuit using a sinusoidal input signal of 1 MHz. Sweep the amplitude of the differential input signal from 1 mV up to 1.5*VDSAT.
   a. Attach the output of the amplifier to an ideal voltage source with a proper value to measure the transconductance gain (output current rather than output voltage). Plot the RMS value of the fundamental tone of the current and the RMS value of the third harmonic component as function of the RMS value of the input signal. Ask your TA for instructions on simulating THD.
   b. Compare this plot with the results obtained from the expression $HD3=(1/32)(V_{in-peak}/VDSAT)^2$

d) Compute the output and input referred noise as function of frequency; identify both flicker and thermal noise components and extract from your simulation the flicker coefficient for this technology. Be sure that flicker noise coefficients are included in cadence models.

Hints:
Before you run the simulations think twice about your simulation set-up.
In case something is not clear, ask instructor or TAs for clarifications.