Agenda

• MOS Transistor Modeling
  • Large-Signal “DC” Model
  • Small-Signal “AC” Model
  • MOS Capacitors

• Current Reading
  • Razavi Chapters 2 & 17
Drawn & Effective Channel Lengths

The transistor gate overlaps both the source and drain region by a length of $L_D$ due to side diffusion in the fabrication process.

This results in the effective transistor gate length, $L_{\text{eff}}$, being shorter than the drawn length, $L_{\text{drawn}}$.

Throughout the remainder of the course, $L$ will generally refer to $L_{\text{eff}}$.

$$L_{\text{eff}} = L_{\text{drawn}} - 2L_D$$

[Image: Diagram showing the overlap of the transistor gate with the source and drain regions.]
Finite Output Resistance in Saturation

- In saturation, as $V_{DS}$ is increased the channel pinch-off point moves slightly towards the source.

- This phenomenon is called channel-length modulation and is characterized by a parameter $\lambda$. 

\[ \lambda = \frac{v_{DS} - v_{OV}}{L'} \]

\[ L' = L - \Delta L \]
Finite Output Resistance in Saturation

- The current will increase slightly with $V_{DS}$ in saturation, resulting in a finite incremental output resistance.

- Note, the channel-length modulation parameter $\lambda$ is inversely proportional to $L$.

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L - \Delta L} (V_{GS} - V_{Tn})^2$$

$$= \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{1}{1 - \frac{\Delta L}{L}} (V_{GS} - V_{Tn})^2$$

$$\approx \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{Tn})^2 \left(1 + \frac{\Delta L}{L}\right)$$

$$\Delta L = \lambda' V_{DS}$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{Tn})^2 \left(1 + \frac{\lambda' V_{DS}}{L}\right)$$

$$\lambda = \frac{\lambda'}{L}$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{Tn})^2 \left(1 + \lambda V_{DS}\right)$$

[Sedra/Smith]
MOS “Large-Signal” Output Characteristic with Finite Output Resistance

\[ \lambda \text{ has units of } V^{-1} \]

\[ -V_A = -1/\lambda \]

Triode: \[ I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn} - 0.5V_{DS}) V_{DS} \]

Saturation: \[ I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{Tn})^2 (1 + \lambda V_{DS}) \]
MOS “Large-Signal” Transfer Characteristic

\[ v_{DS} \geq v_{GS} - V_{tn} \]

\[ I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{tn})^2 (1 + \lambda V_{DS}) \]

\[ 0 \quad V_{tn} \]

\[ v_{GS} \]

\[ 0 \]

\[ v_{OV} \]
Impact of Bulk Voltage

\[ I_D = \frac{\mu_n C_{ox} W}{2 L} (V_{GS} - V_{Tn})^2 (1 + \lambda V_{DS}) \]

\[ V_T = V_{T0} + \gamma \left[ \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right] \rightarrow V_T \big|_{V_{SB}=0} \]

- The current decreases as \( V_{SB} \) increases due to an increased threshold voltage
Large-Signal “DC” Response

\[ v_O = V_{DC} = V_{DD} - I_{DS}R \]
Large-Signal “DC” + Small-Signal “AC” Response

- For small-signal analysis, we “linearize” the response about the DC operating point.
- If the signal is small enough, linearity holds and the complete response is the summation of the large-signal “DC” response and the small-signal “AC” response.

\[ V_{\text{out}} = V_{\text{DC}} + V_{\text{AC}} = (V_{\text{DD}} - I_{\text{DSR}}) - i_{\text{ds}} R \]
The linearized small-signal model is formed by computing an effective voltage-to-current transformation factor “conductance” by differentiating the large-signal response at the DC operating point.

\[ i_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} v_{gs} + \frac{\partial I_{ds}}{\partial V_{bs}} v_{bs} + \frac{\partial I_{ds}}{\partial V_{ds}} v_{ds} \]

\[ i_{ds} = g_m V_{gs} + g_{mb} V_{bs} + g_{ds} V_{ds} \]
Transconductance, $g_m$

- Transistor transfer characteristic is used to extract transconductance, $g_m$

In Saturation (Neglecting $\lambda$ Effects)

$$I_D = \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} (V_{GS} - V_T)^2$$

$$g_m = \left. \frac{\partial i_D}{\partial v_{gs}} \right|_Q = \mu C_{OX} \frac{W}{L_{eff}} (V_{GS} - V_T)$$

[Sedra/Smith]
Output Conductance, $g_o$

- Transistor output characteristic is used to extract output conductance, $g_o$.

In Saturation (Including $\lambda$ Effects)

$$I_D = \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$g_o = \frac{\partial i_D}{\partial v_{ds}} \bigg|_Q = \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} (V_{GS} - V_T)^2 \lambda \bigg|_Q \approx \lambda I_D$$
Body Transconductance, $g_{mb}$

- The small-signal drain current changes with $V_{BS}$ modulation due to changes in $V_T$

$$g_{mb} = \frac{\partial i_D}{\partial v_{bs}} = \mu C_{OX} \left( \frac{W}{L_{eff}} (V_{GS} - V_T) \right) \left( -\frac{\partial V_T}{\partial v_{bs}} \right) = \frac{\gamma g_m}{2\sqrt{2\phi_F + V_{SB}}}$$. 

In Saturation (Neglecting $\lambda$ Effects)
Low-Frequency Small-Signal Model

\[ i_{ds} = g_m V_{gs} + g_{mb} V_{bs} + g_{ds} V_{ds} \]

\[ g_m = \left. \frac{\partial i_D}{\partial v_{gs}} \right|_Q = \mu_{COX} \frac{W}{L_{eff}} \left( V_{GS} - V_T \right) \]

\[ g_0 = \left. \frac{\partial i_D}{\partial v_{ds}} \right|_Q = \left( \frac{\mu_{COX}}{2} \right) \left( \frac{W}{L_{eff}} \left( V_{GS} - V_T \right) \right)^2 \]

\[ g_{mb} = \left. \frac{\partial i_D}{\partial v_{bs}} \right|_Q = \mu_{COX} \frac{W}{L_{eff}} \left( V_{GS} - V_T \right) \left( \frac{\partial V_T}{\partial v_{bs}} \right)_Q \]

\[ g_{mb} = \frac{g_m}{2 \sqrt{2 \phi_F + V_{SB}}} \]
MOS Transistor Capacitances

Gate - Channel Cap = $C_{GC} = W L_{eff} C_{ox}$

Channel - Bulk Cap = $C_{CB} = W L_{eff} \sqrt{q \varepsilon_{Si} N_{sub} \over 4 \Phi_F}$

Gate - Source Overlap (Fringing) Cap = $C_{GSo} = W C_{ov}$ Note, $C_{ov} \neq C_{ox} L_D$

Gate - Drain Overlap (Fringing) Cap = $C_{GDov} = W C_{ov}$

Source - Bulk Junction Cap = $C_{SBJ} = A_S C_j + P_S C_{jsw}$

Drain - Bulk Junction Cap = $C_{DBJ} = A_D C_j + P_D C_{jsw}$

\[
C_j = \frac{C_{j0} \left(1 + \frac{V_{BX}}{\Phi_B}\right)^m}{m} \quad C_{jsw} = \frac{C_{jsw0} \left(1 + \frac{V_{BX}}{\Phi_B}\right)^{msw}}{msw}
\]
MOS Transistor Capacitances (Off)

[Razavi]

Gate - Drain Cap = \( C_{GD} = C_{GDOv} = WC_{ov} \)

Gate - Source Cap = \( C_{GS} = C_{GDOv} = WC_{ov} \)

Gate - Bulk Cap = \( C_{GB} = \frac{C_{GC}C_{CB}}{C_{GC} + C_{CB}} \)

Drain - Bulk Cap = \( C_{DB} = C_{DBJ} \)

Source - Bulk Cap = \( C_{SB} = C_{SBJ} \)
MOS Transistor Capacitances (Triode)

[Image of MOS transistor diagram]

\[
\begin{align*}
\text{Gate - Drain Cap} &= C_{GD} = C_{GDov} + \frac{1}{2} C_{GC} \\
\text{Gate - Source Cap} &= C_{GS} = C_{Gsov} + \frac{1}{2} C_{GC} \\
\text{Gate - Bulk Cap} &= C_{GB} \approx 0 \\
\text{Drain - Bulk Cap} &= C_{DB} = C_{DBJ} + \frac{1}{2} C_{CB} \\
\text{Source - Bulk Cap} &= C_{SB} = C_{SBJ} + \frac{1}{2} C_{CB}
\end{align*}
\]
MOS Transistor Capacitances (Saturation)

Gate - Drain Cap = $C_{GD} = C_{GDoV}$

Gate - Source Cap = $C_{GS} = C_{GSov} + \frac{2}{3} C_{GC}$

Gate - Bulk Cap = $C_{GB} \approx 0$

Drain - Bulk Cap = $C_{DB} = C_{DBJ}$

Source - Bulk Cap = $C_{SB} = C_{SBJ} + \frac{2}{3} C_{CB}$
MOS Gate Capacitors Response

Note, $C_{ov} \neq C_{ox}L_D$
MOS Source & Drain Junction Capacitors

\[ A_S = A_D = WE \]

\[ P_S = P_D = 2(W + E) \]

Junction \( C_{SB} = C_{DB} = AC_j + PC_{jsw} = WEC_j + 2(W + E)C_{jsw} \)
Source/Drain Junction Perimeter Caps

Disclaimer

• Note, there is some ambiguity on how to model the source/drain junction perimeter (sidewall) capacitance on the side of the gate
  • This is due to the channel occupying a portion of the sidewall area
  • Different textbooks present different approaches

• The Razavi text conservatively assumes that the sidewall perimeter capacitance is the same on all sides

• The Johns/Martin text (sometimes previously used) optimistically sets the sidewall perimeter cap to zero under the gate

• The correct answer is somewhere in the middle

• We will follow the Razavi method and assume that the sidewall perimeter capacitance is the same on all sides (even under the gate)
  • I will try to make it clear on any problem description
Folding the transistor allows for approximately half the drain junction capacitance with a small increase in source junction capacitance.
Other resistors: Source/Drain

Drain/Source Resistance

In addition to the contact resistance, the diffusion resistance has to be considered.

\[ R_{\text{series}} = \frac{L_R}{W} \left( R_{||} \right) \]

• In SPICE, \( R_{||} \) is defined as RSH
Small Signal Model (Saturation region)

\[ I_D = \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} [V_{GS} - V_T] [1 + \lambda V_{DS}] \]

\[ V_T = V_{T0} + \gamma \left[ \sqrt{2 \phi_F + V_{SB}} - \sqrt{2 \phi_F} \right] \]

\[ i_D \approx \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} [V_{GS} - V_T] [1 + \lambda V_{DS}] \bigg|_Q + \frac{\partial i_D}{\partial v_{gs}} \bigg|_Q v_{gs} + \frac{\partial i_D}{\partial v_{ds}} \bigg|_Q v_{ds} + \frac{\partial i_D}{\partial v_{bs}} \bigg|_Q v_{bs} \]

\[ i_D \approx I_D + g_m v_{gs} + g_0 v_{ds} + g_{mb} v_{bs} \]
Next Time

- MOS Transistor Modeling
  - High-Field “Short-Channel” Effects
  - Spice Models