ECEN474/704: (Analog) VLSI Circuit Design
Spring 2018

Lecture 6: Current Mirrors

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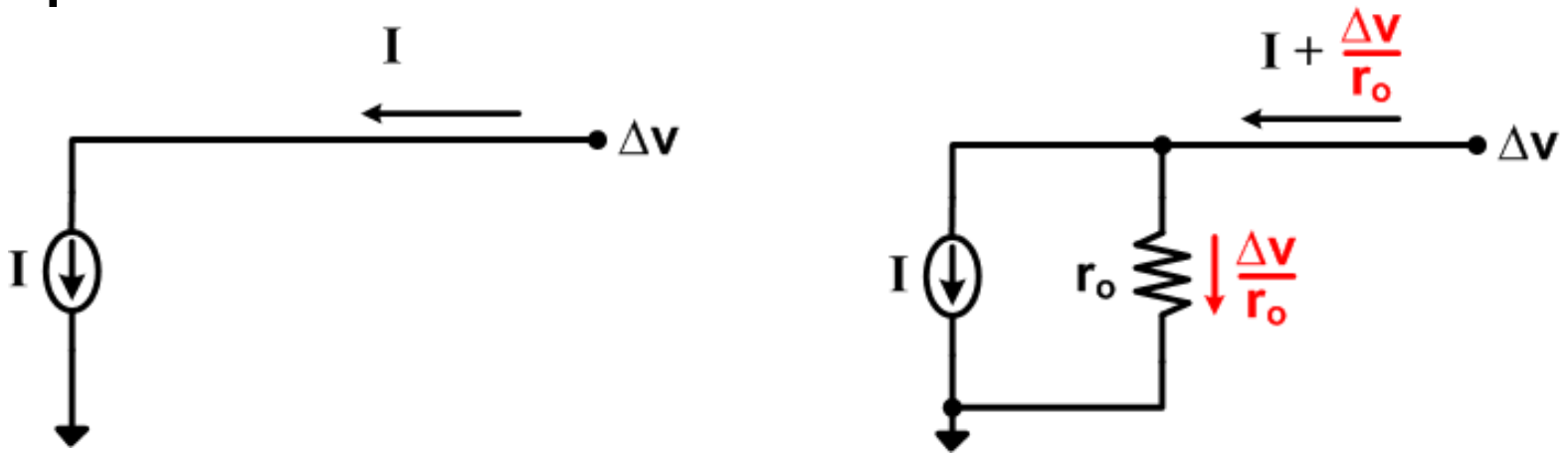
Announcements & Agenda

- Reading
  - Razavi Chapter 5

- Biasing in ICs
- Simple Current Mirror
- Cascode Current Mirror
- Low-Voltage Cascode Current Mirror

Current Source Properties

- Output Resistance



  - Finite output resistance degrades current source accuracy and amplifier gain
- Other important properties:
  - Voltage headroom (compliance voltage)
  - Accuracy
  - Noise

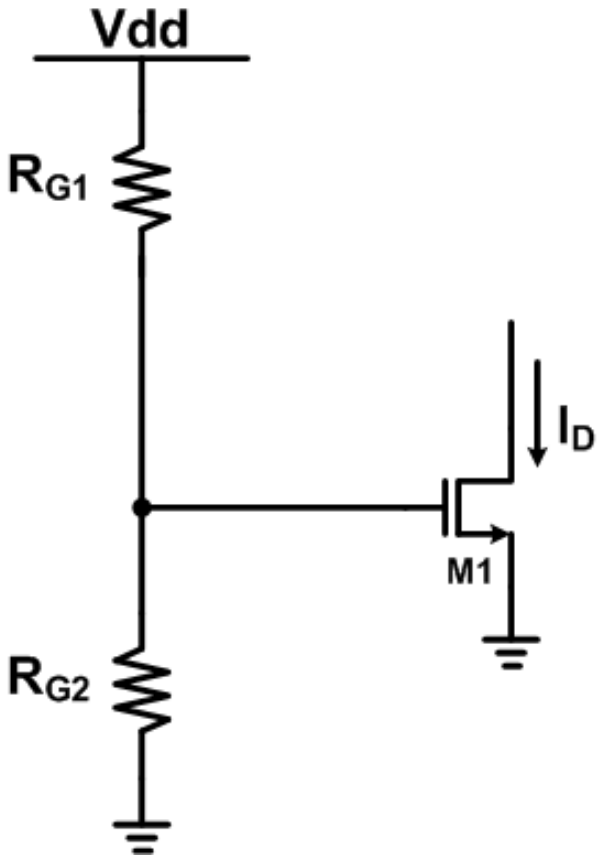
How Should We Bias Our Circuits?

- Resistive Biasing
  - Assuming saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G - V_{Tn})^2$$

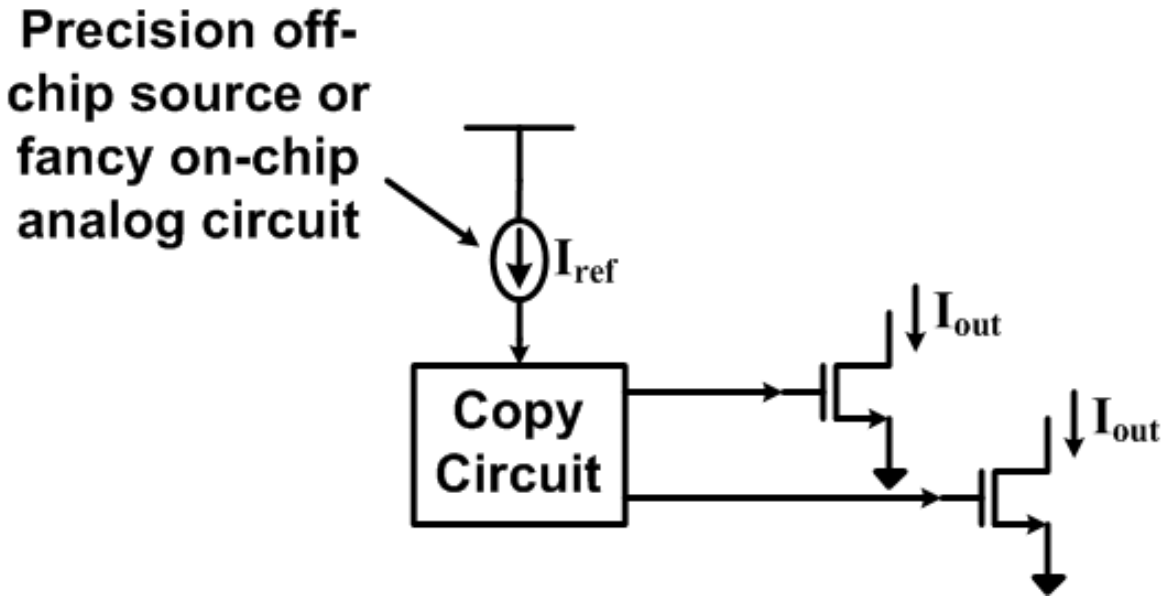
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_{G2}}{R_{G1}+R_{G2}}Vdd - V_{Tn}\right)^2$$

- I_D is sensitive to
  - Supply (Vdd)
  - Process (V_{Tn} and $\mu_n C_{ox} W/L$)
  - Temperature (V_{Tn} and μ_n)



IC Biasing

- In IC design we often assume that we have **one** precise current source and we copy its value to our circuits



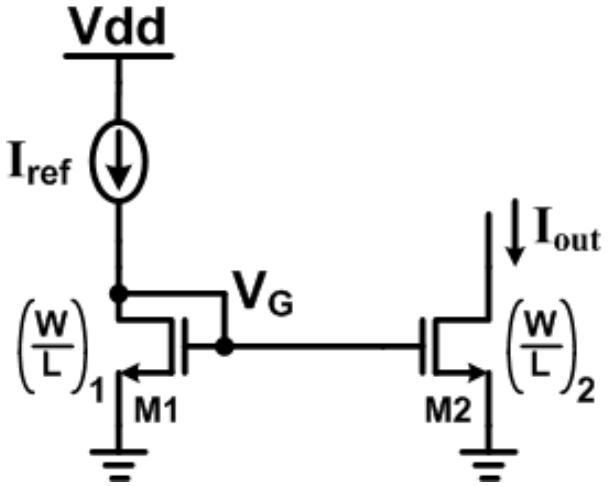
Simple Current Mirror

- That copy circuit is a current mirror
- Simple Current Mirror

What is V_G ?

$$I_D = I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_G - V_{Tn})^2$$

$$V_G = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn}$$

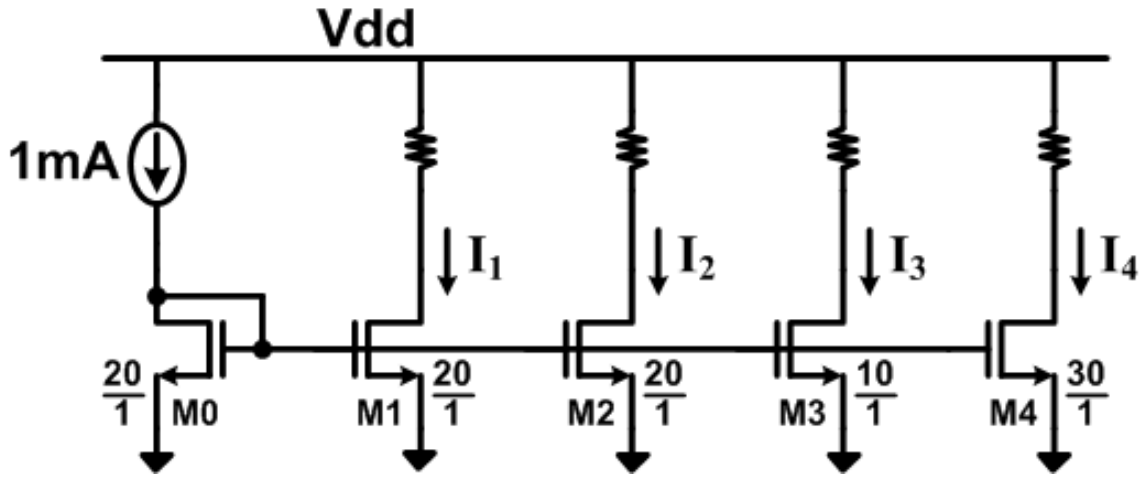


- If VG is applied to another transistor

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn} - V_{Tn}\right)^2$$

$$\Rightarrow \quad \boxed{I_{out} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{REF}}$$

Ideal Current Mirror Example



I_1=1mA

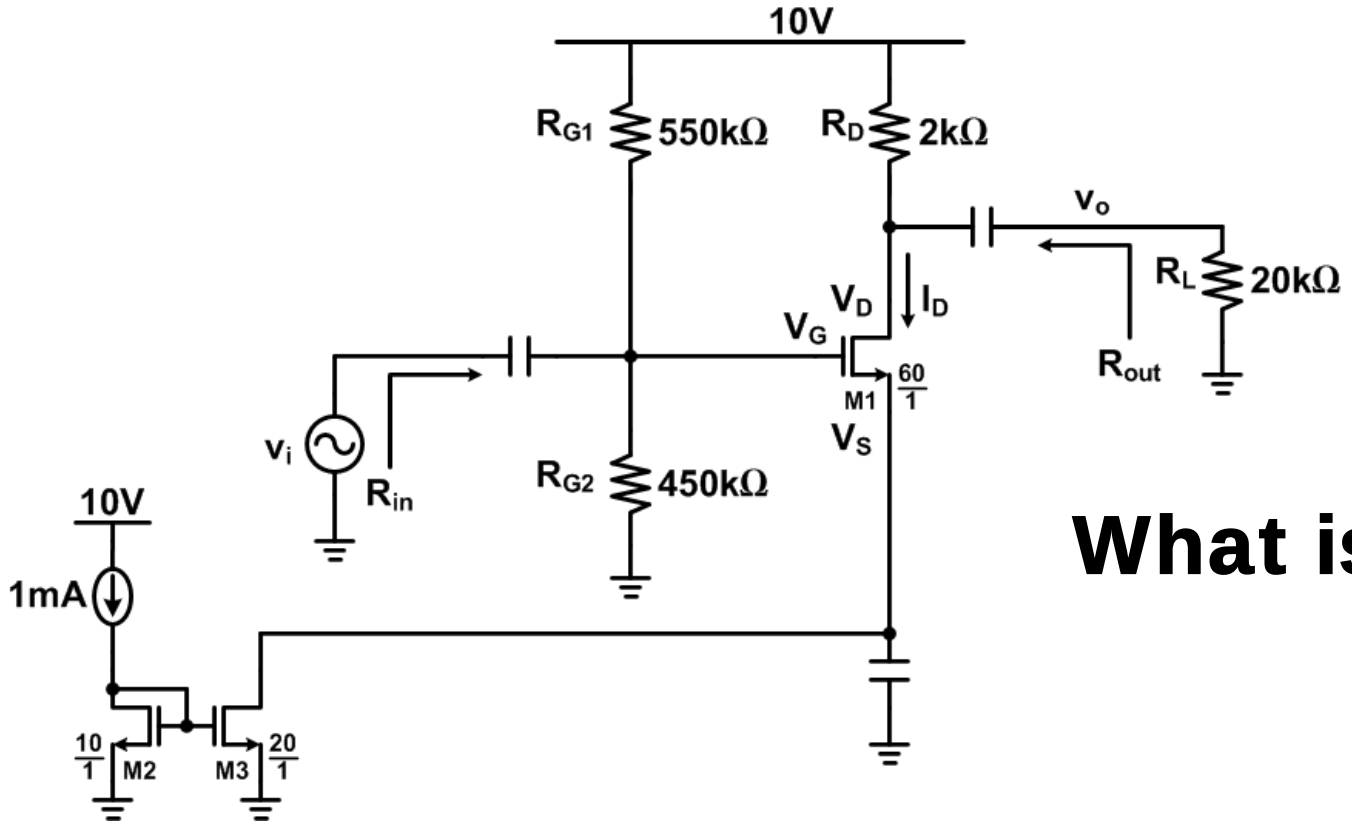
I_2=1mA

I_3=0.5mA

I_4=1.5mA

- This bias scheme reduces sensitivity to process, voltage, and temperature variations

CS Amplifier w/ Current Source

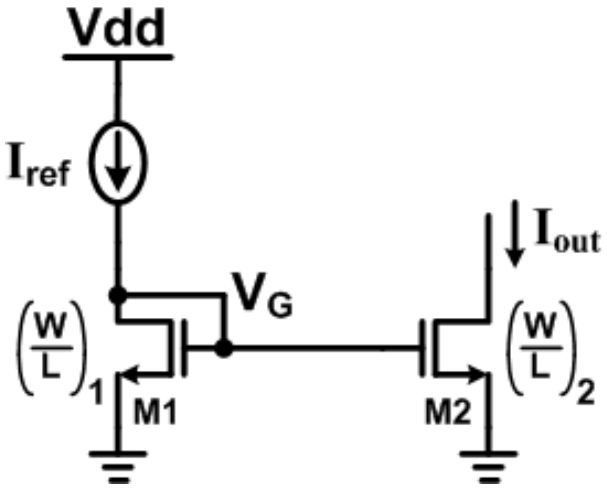


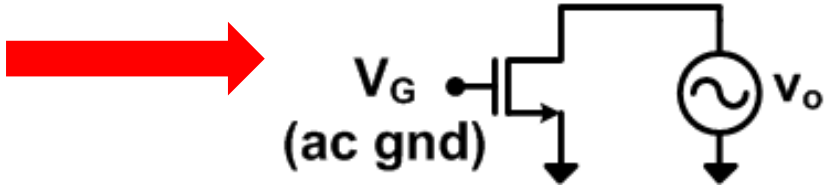
What is I_D?

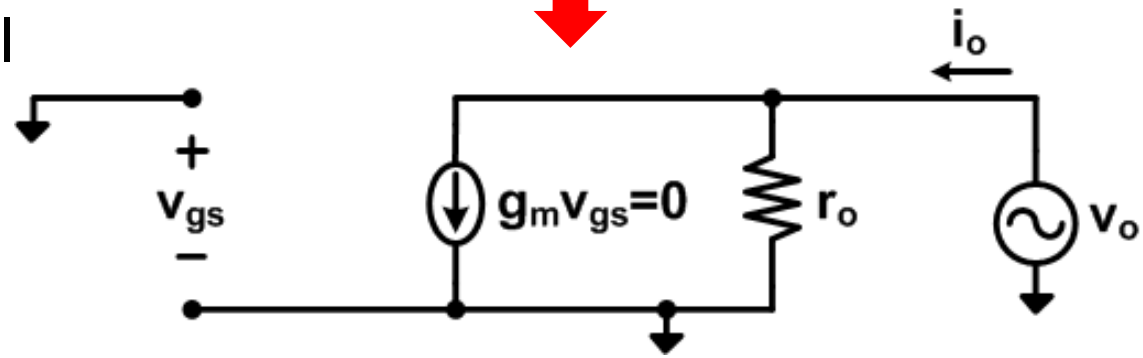
- Need to insure that M3 remains in saturation

$$V_s = V_G - (V_{ov1} + V_{Tn}) = \left(\frac{R_{G2}}{R_{G1}+R_{G2}}\right)Vdd - \left(\sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn}\right)$$

Small-Signal Output Resistance: Simple Current Mirror/Source (Finite r_o)





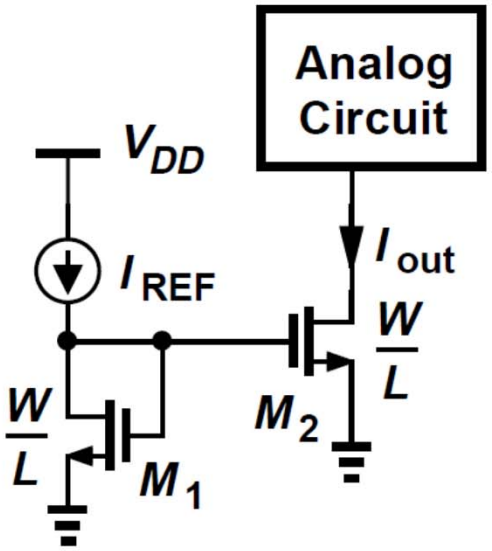


- A simple current mirror/source has an output resistance equal to a single transistor r_o
- In order to maintain a high output impedance we need a minimum output compliance voltage

$$\text{Compliance Voltage} = V_{DSAT2} = V_{GS2} - V_{T2}$$

$$r_{out} = \frac{1}{g_o}$$

Simple Current Mirror Accuracy



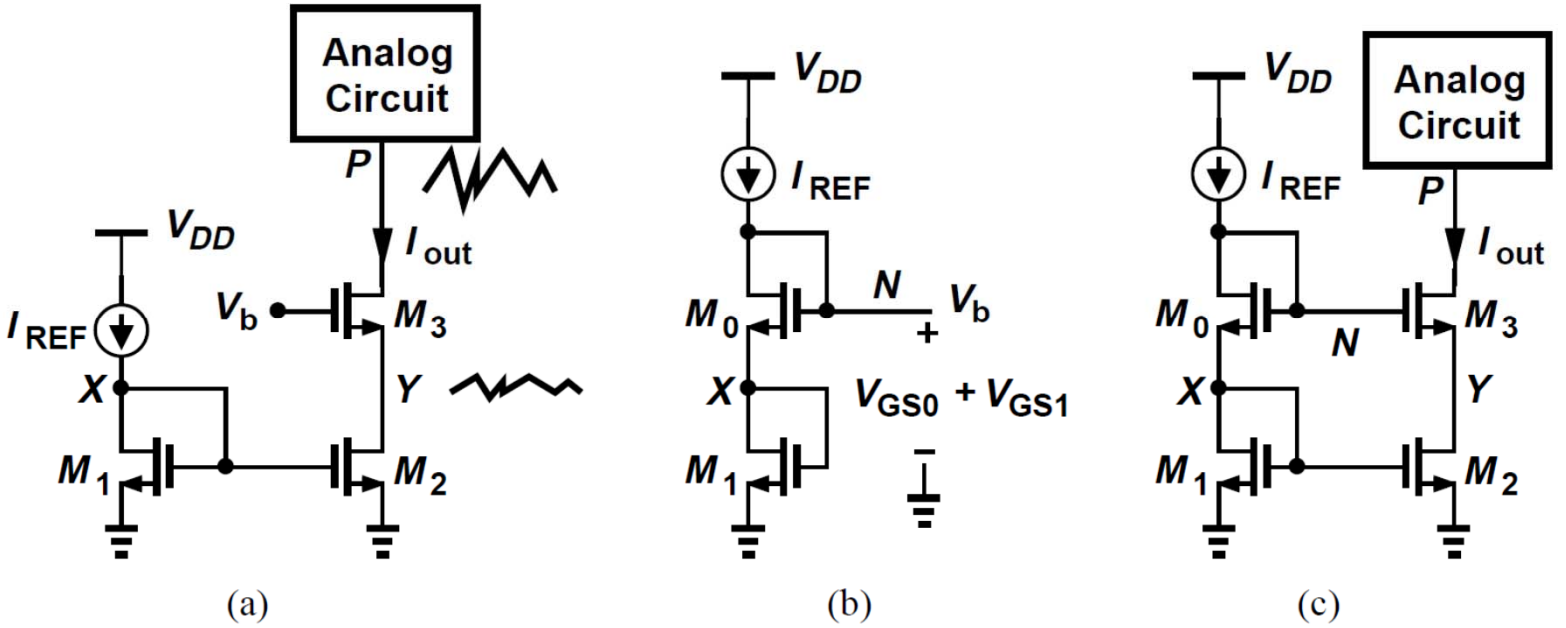
$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}.$$

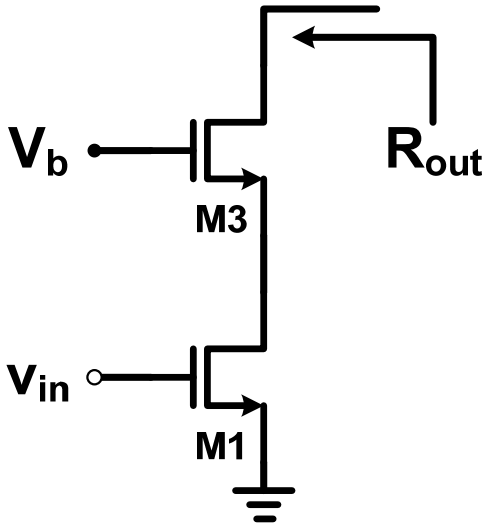
- While $V_{DS1}=V_{GS1}=V_{GS2}$, V_{DS2} may not equal V_{DS1}
  - This causes an error in the mirroring ratio
- To improve accuracy we can (a) force V_{DS2} to be equal to V_{DS1} (Cascode Current Mirror), or (b) force V_{DS1} to be equal to V_{DS2} (Low-Voltage Cascode Current Mirror)

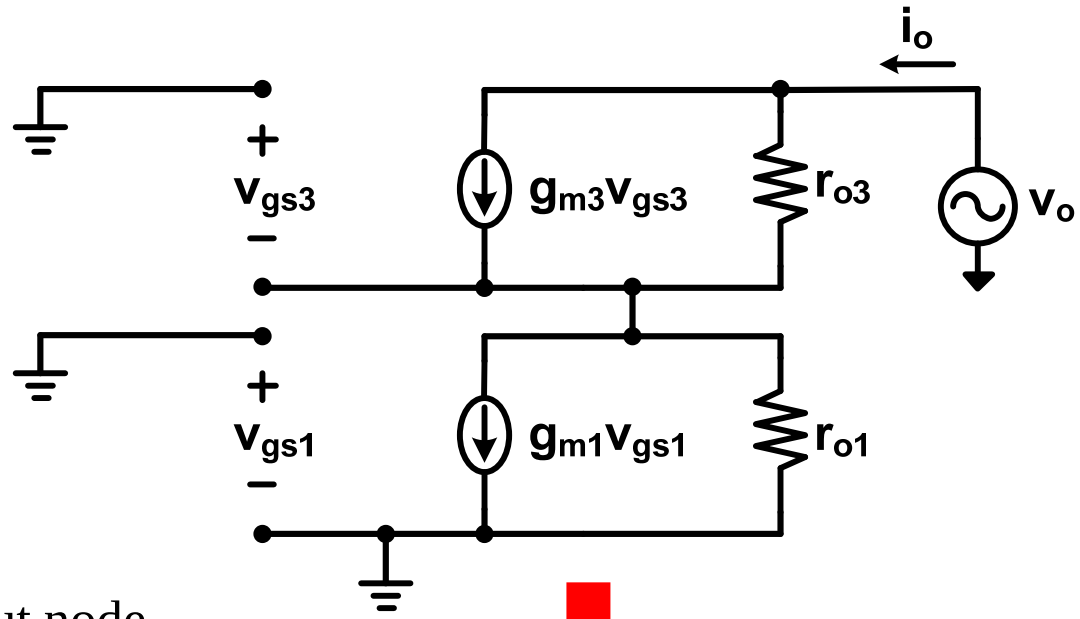
Cascode Current Mirror



- A cascode device can shield a current source, thereby reducing the voltage variations across it.
- But, how do we ensure that $V_{DS2} = V_{DS1}$?
- We can generate V_b such that $V_b - V_{GS3} = V_{DS1} (= V_{GS1})$ with a stacked diode connected transistor

MOS Cascode Topology Output Resistance





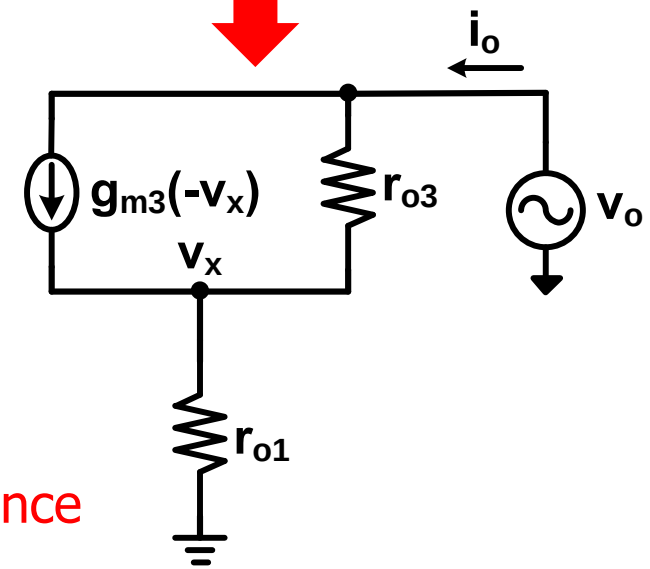
$$v_x = i_o r_{o1}$$

Writing a KCL at the output node

$$-i_o + g_{m3}(-v_x) + \frac{v_o - v_x}{r_{o3}} = 0$$

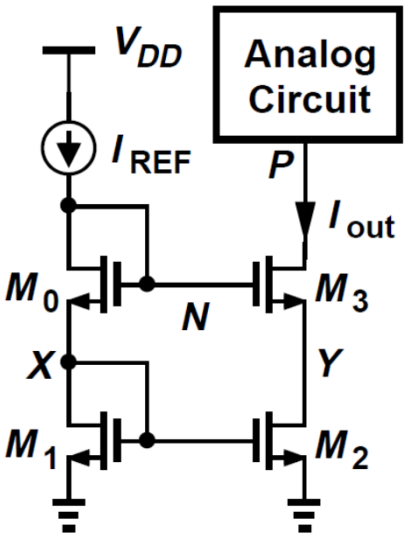
$$-i_o - g_{m3} i_o r_{o1} - \frac{i_o r_{o1}}{r_{o3}} = -\frac{v_o}{r_{o3}}$$

$$R_{out} = \frac{v_o}{i_o} = r_{o3} + r_{o1} + g_{m3} r_{o3} r_{o1} \approx g_{m3} r_{o3} r_{o1}$$



The dominant term is the bottom effective resistance boosted by the gain of the top transistor ($g_{m3}r_{o3}$)

Cascode Current Mirror Compliance Voltage



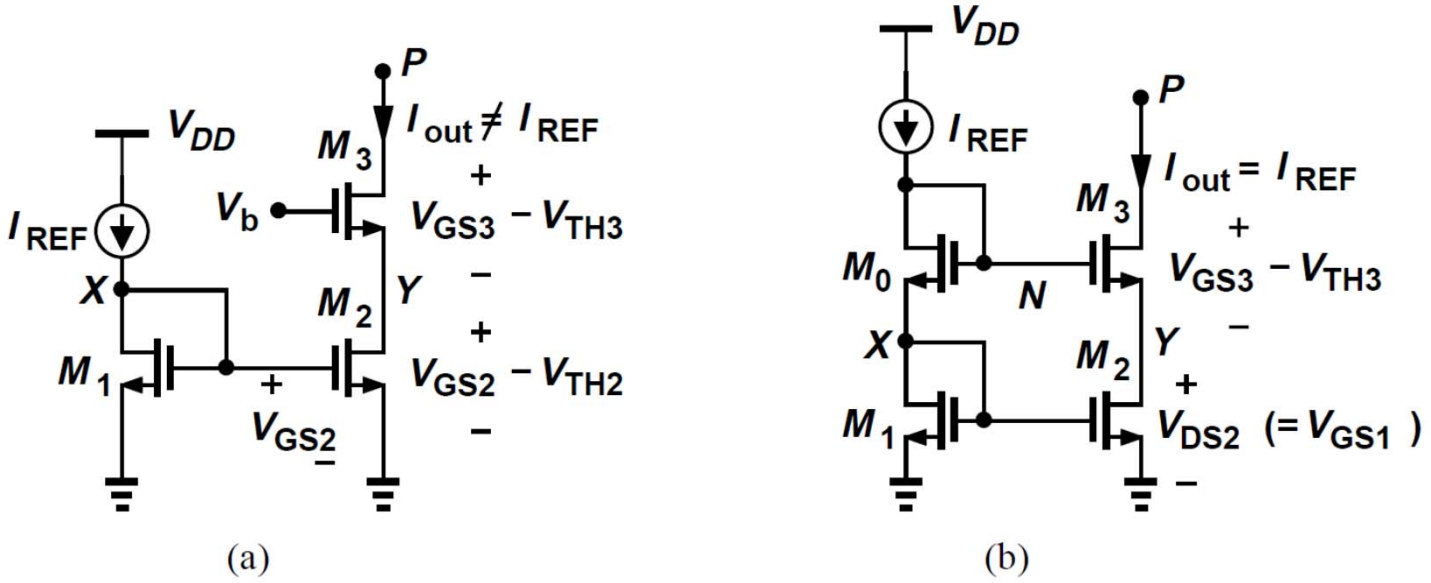
- What is the minimum output voltage V_P such that all the output transistors remain in saturation?

$$V_P = V_Y + V_{DSAT3} = V_{GS1} + V_{GS3} - V_T$$

$$\boxed{\text{Compliance Voltage} = V_{GS1} + V_{DSAT3}}$$

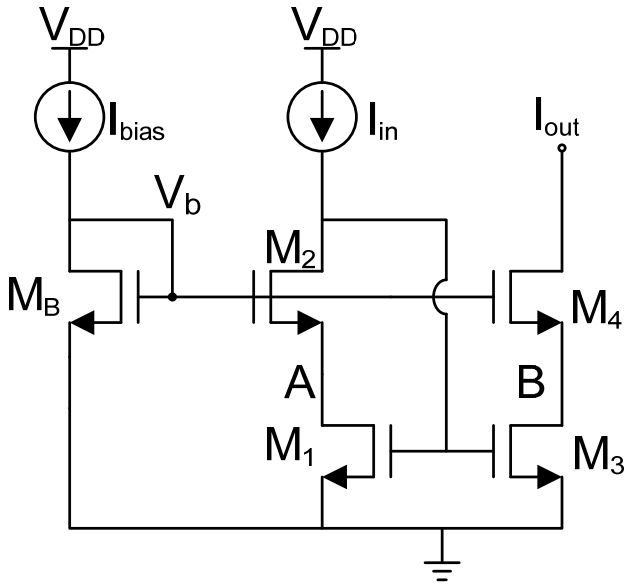
- Note that this output stage biasing technique "wastes" one threshold voltage, as V_Y could potentially be lower by a V_T and M_2 would still be in saturation

How Can We Get a Lower Compliance Voltage?



- The left figure uses the minimum possible V_b such that M_2 and M_3 remain in saturation
  - However, as $V_X \neq V_Y$, the output current does not accurately track I_{REF}
- The right figure (our original cascode current mirror) achieves good accuracy, but again wastes a threshold voltage relate to the left figure

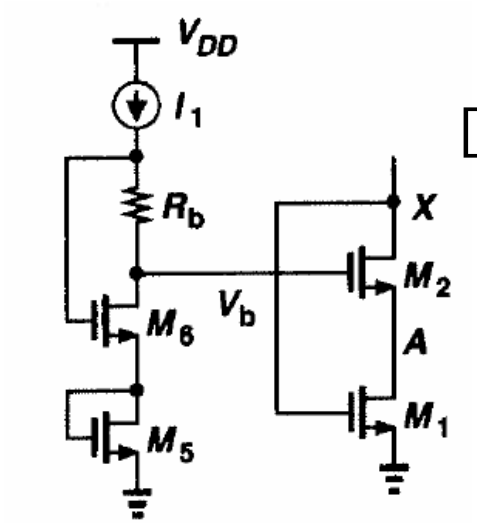
Low-Voltage Cascode Current Mirror



Compliance Voltage $= V_{DSAT3} + V_{DSAT4}$

- M2 and M4 should be sized such that
  - $V_{GS2} = V_{GS4}$
- M1 and M3 biased near edge of saturation
  - $V_{DS1} \approx V_{DS3} \approx V_{DSAT}$
  - $V_b = V_{GS2}+(V_{GS1}-V_{T1}) = V_{GS4}+(V_{GS3}-V_{T3})$

Alternative V_b Generation



[Razavi]

- Saves one current branch
- M5 sized such that $V_{GS5} \approx V_{GS2}$
  - Some body effect error here
- Size M6 and Rb such that
  - $V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{T1}$

Next Time

- Table-Based Design