Lecture 6: Table-Based \((g_m/I_D)\) Design
Announcements

• Exam 1 is on 9/29
  • **It will be in WEB 236C**
  • 2:20-3:45PM (10 extra minutes)
  • Closed book w/ one standard note sheet
  • 8.5”x11” front & back
  • Bring your calculator
  • Covers material through lecture 5
  • Previous years’ exam 1s are posted on the website for reference

• Reading
  • $g_m/I_D$ paper and book reference on website
    • Material is only supplementary reference
  • Razavi Chapter 5 (Current Mirrors)
Agenda

- Technology characterization for design
- Table-based \((g_m/I_D)\) design example
- Adapted from Prof. B. Murmann (Stanford) notes
How to Design with Modern Sub-Micron (Nanometer) Transistors?

• Hand calculations with square-law model can deviate significantly from actual device performance
  • However, advanced model equations are too tedious for design

• Tempts designers to dive straight to simulation with little understanding on circuit performance trade-offs
  • “Spice Monkey” approach

• How can we accurately design when hand analysis models are way off?

• Employ a design methodology which leverages characterization data from BSIM simulations
The Problem

Specifications

Square Law → Hand Calculations

BSIM → Circuit

Spice

Results

[Murmann]
The Solution

BSIM → Spice → Design Charts → Hand Calculations → Circuit → BSIM → Spice → Results

[Murmann]
Technology Characterization for Design

• Generate data for the following over a reasonable range of $g_m/I_D$ and channel lengths
  • Transit frequency ($f_T$)
  • Intrinsic gain ($g_m/g_{ds}$)
  • Current density ($I_D/W$)
• Also useful is extrinsic capacitor ratios
  • $C_{gd}/C_{gg}$ and $C_{dd}/C_{gg}$
• Parameters are (to first order) independent of transistor width, which enables “normalized design”
• Do design hand calculations using the generated technology data
• Still need to understand how the circuit operates for an efficient design!!!
$g_m/I_D$

- These plots tell us how much transconductance ($g_m$) we can get for a given current ($I_D$)
- The transistor is a more efficient transconductor at low overdrive voltages
- A main trade-off will be the transistor frequency response ($f_T$)
- We will use $g_m/I_D$ as the reference axis to compare other transistor parameters

NMOS $g_m/I_D$ vs $V_{ov}$, $W=6\,\mu m$, $V_{DS}=1.5\,V$
Intrinsic Transistor Gain (gm/go)

These plots tell us how much intrinsic transistor gain we have.

The transistor has higher intrinsic gain at lower overdrive values due to the output resistance decreasing faster than the transconductance increases at higher current levels.

Plotted vs gm/ID shows that after a certain minimum level, the transistor gain is somewhat flat.
Transit Frequency, $f_T$

The transit frequency is defined as the frequency when the transistor small-signal current gain goes to unity with the source and drain at AC grounds.

Overall, the ratio of $g_m$ to $C_{gg}$ comes up often in analog circuits, and is a good metric to compare the device frequency response (speed).

Transistor $f_T$ increases with overdrive voltage and high $f_T$ values demand a low $g_m/I_D$.

If you need high bandwidth, you have to operate the device at low efficiency.

\[
f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} = \frac{g_m}{2\pi C_{gg}}
\]
• Ultimately, we need to know how to size our devices to get a certain current
• The current density of a transistor increases with increased VGS or overdrive voltage
• High gm/ID requires low current density, which implies bigger devices for a given current
CS Amplifier Design Example

- Specifications
  - 0.6μm technology
  - $|A_v| \geq 4V/V$
  - $f_u \geq 100$MHz
  - $C_L = 5pF$
  - $V_{dd} = 3V$
CS Amplifier Small-Signal Model (No $R_S$)

\[
\frac{v_o}{v_i} = \frac{(sC_{gd} - g_m)R_\parallel}{s(C_L + C_{gd} + C_{db})R_\parallel + 1}, \quad \text{where } R_\parallel = \frac{r_o R_L}{r_o + R_L}
\]

\[
\omega_z = \frac{g_m}{C_{gd}} \quad \text{(located at very high frequency, } > \omega_T \text{)}
\]

\[
\omega_p = -\frac{1}{R_\parallel(C_L + C_{gd} + C_{db})} \approx -\frac{1}{R_L C_L}
\]

\[
A_v = -g_m R_\parallel \approx -g_m R_L
\]

\[
\omega_u = A_v \omega_p \approx \frac{g_m}{C_L}
\]
Design Procedure

1. Determine $g_m$ from design specifications
   a. $\omega_u$ in this example

2. Pick transistor L
   a. Short channel $\rightarrow$ high $f_T$ (high bandwidth)
   b. Long channel $\rightarrow$ high $r_o$ (high gain)

3. Pick $g_m/I_D$ (or $f_T$)
   a. Large $g_m/I_D$ $\rightarrow$ low power, large signal swing (low $V_{ov}$)
   b. Small $g_m/I_D$ $\rightarrow$ high $f_T$ (high speed)
   c. May also be set by common-mode considerations

4. Determine $I_D/W$ from $I_D/W$ vs $g_m/I_D$ chart

5. Determine $W$ from $I_D/W$

• Other approaches exist
1. Determine $g_m$ (& $R_L$)

- From $\omega_u$ and DC gain specification

$$\omega_u = A_v \omega_p \approx \frac{g_m}{C_L}$$

$$g_m = \omega_u C_L = 2\pi (100\,MHz)(5\,pF) = 3.14\,mA/V$$

Note, this may be slightly low due to neglecting $C_{gd}$ and $C_{db}$

$$A_v = -g_m R_\parallel \approx -g_m R_L$$

$$R_L = \frac{A_v}{g_m}$$

Adding 20% margin to compensate for $r_o$ effects

$$R_L = \frac{A_v}{g_m} = \frac{4.8}{3.14\,mA/V} = 1.5\,k\Omega$$
2. Pick Transistor L

- Need to look at gain and $f_T$ plots

NMOS Gain ($g_m / g_0$) vs $g_m / I_D$, $W=6\mu m$, $V_{DS}=1.5V$

$g_m / I_D$ vs $g_m / I_D$ for $L=0.6\mu m$, $L=1.2\mu m$, $L=2.4\mu m$

NMOS $f_T$ ($g_m / C_{gg}$) vs $g_m / I_D$, $W=6\mu m$, $V_{DS}=1.5V$

$g_m / I_D$ vs $g_m / I_D$ for $L=0.6\mu m$, $L=1.2\mu m$, $L=2.4\mu m$

- Since amplifier $A_v \geq 4$, min channel length ($L=0.6\mu m$) will work with $g_m / I_D \rightarrow 2$
  - Min channel length provides highest $f_T$ at this $g_m / I_D$ setting
3. Pick \( g_m/I_D \) (or \( f_T \))

- Setting \( I_D \) for \( V_O=1.5V \) for large output swing range.

\[
I_D = \frac{3V - 1.5V}{1.5k\Omega} = 1mA
\]

\[
g_m = \frac{3.14mA/V}{1mA} = 3.14V^{-1}
\]
Verify Transistor Gain & $f_T$ at $g_m/l_D$ Setting

- Transistor gain = 30.6 >> amplifier $A \geq 4$
- Transistor $f_T = 6.7$GHz >> amplifier $f_u = 100$MHz
- $g_m/l_D$ setting is acceptable
4. Determine Current Density ($I_D/W$)

- $g_m/I_D = 3.14V^{-1}$ maps to a current density of $20.2\mu A/\mu m$

- Verify current density is achievable at a reasonable $V_{GS}$

- $V_{GS} = 1.15V$ is reasonable with $V_{dd} = 3V$ & $V_{DS} = 1.5V$
5. Determine Transistor $W$ from $\frac{I_D}{W}$

- From Step 3, we determined that $I_D = 1mA$

$$W = \frac{I_D}{(I_D/W)} = \frac{1mA}{\frac{20.2 \mu A/\mu m}{49.5 \mu m}} = 49.5 \mu m$$

- For layout considerations and to comply with the technology design rules
  - Adjust 49.5$\mu m$ to 49.2$\mu m$ and realize with 8 fingers of 6.15$\mu m$
  - This should match our predictions well, as the charts are extracted with a 6$\mu m$ device
    - Although it shouldn’t be too sensitive to exact finger width
### Operating Point Information

**Design Value**

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**Total Cgate = Cgg = 74.1fF**

**Total Cdrain = Cdd + Cjd = 12.5fF + 55.6fF = 68.1fF**

**Total Csource = Css + Cjs = 43.2fF + 0fF = 43.2fF**
AC Response

- Design is very close to specs
- Discrepancies come from neglecting $r_o$ and $C_{\text{drain}}$
- With design table information we can include estimates of these in our original procedure for more accurate results

$A_v = 12.2\,\text{dB} = 4.07\,\text{V/V}$

$f_u = 95.5\,\text{MHz}$
Next Time

• Current Mirrors