Announcements & Agenda

• HW2 due Mar 9

• Reading
  • Razavi Chapter 5

• Biasing in ICs

• Simple Current Mirror

• Transistor Small-Signal Impedances
  • Simple Amplifiers

• Other Current Mirror Topologies
Current Source Properties

• Output Resistance

![Diagrams showing output resistance and finite output resistance effects]

• Finite output resistance degrades current source accuracy and amplifier gain

• Other important properties:
  • Voltage headroom (compliance voltage)
  • Accuracy
  • Noise
How Should We Bias Our Circuits?

- Resistive Biasing
  - Assuming saturation

\[
I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( V_G - V_{Tn} \right)^2
\]

\[
= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( \frac{R_{G2}}{R_{G1} + R_{G2}} Vdd - V_{Tn} \right)^2
\]

- \( I_D \) is sensitive to
  - Supply (Vdd)
  - Process \((V_{Tn} \text{ and } \mu_n C_{ox} W/L)\)
  - Temperature \((V_{Tn} \text{ and } \mu_n)\)
IC Biasing

• In IC design we often assume that we have **one** precise current source and we copy its value to our circuits.
Simple Current Mirror

- That copy circuit is a current mirror

**Simple Current Mirror**

What is $V_G$?

$$I_D = I_{REF} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_1 (V_G - V_{Tn})^2$$

$$V_G = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} \left( \frac{W}{L} \right)_1}} + V_{Tn}$$

- If $V_G$ is applied to another transistor

$$I_{out} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_2 \left( \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} \left( \frac{W}{L} \right)_1}} + V_{Tn} - V_{Tn} \right)^2$$

$$I_{out} = \left( \frac{W}{L} \right)^2 I_{REF}$$
Ideal Current Mirror Example

- This bias scheme reduces sensitivity to process, voltage, and temperature variations.
• Need to insure that M3 remains in saturation

\[ V_s = V_G - (V_{ovl} + V_{Tn}) = \left( \frac{R_{G2}}{R_{G1} + R_{G2}} \right) V_{dd} - \left( \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}} + V_{Tn}} \right) \]
Current Mirrors: Accuracy limitations

In general \((W/L)_2=N(W/L)_1\), most probably \(V_{T1}\neq V_{T2}\), then

\[
I_{D2} = \frac{\mu_n C_{OX}}{2} \left(\frac{W}{L}\right) \left(V_{GS} - V_T\right)^2 (1 + \lambda_2 V_{DS2})
\]

\[
I_{D2} = \frac{\mu_n C_{OX}}{2} \left(\frac{W}{L}\right) \left(V_{GS} - V_{T2}\right)^2 (1 + \lambda_2 V_{DS2})
\]

\[
I_{D1} = \frac{K_{P2} (V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})}{K_{P1} (V_{GS} - V_{T1})^2 (1 + \lambda_1 V_{DS1})} \quad \text{NI}_{D1}
\]

Errors can be reduced (but not eliminated) by using replicas of the main device and good layout!

Effective mobility and threshold voltages are sensitive to \(V_{DS}\) and \(V_{dsat}\)

Long devices reduce the error; make \(V_{DS1}=V_{DS2}\)

Good solution \(\Rightarrow\) use cascode structures
DC Current Mirrors: Second-Order Effects

After good layout: Tolerances in N are in the range of 0.5-2 %. Usually mismatches are inversely proportional to gate area!

\[
\frac{I_{D2}}{I_{D1}} = \frac{\mu_2 (V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})}{\mu_1 (V_{GS} - V_{T1})^2 (1 + \lambda_1 V_{DS1})^N}
\]

Mobility degradation

\[
\text{Error} \approx \mu_2 - \mu_1
\]

\[
\mu = \mu_0 \frac{1}{1 + \frac{V_{gs}}{\theta V_{gs}}} \frac{1}{1 + \frac{V_{ds}}{L \varepsilon_{\text{crit}}}}
\]

Error is minimized by using replicas of the basic device

Intra-die \(V_T\) mismatches are inversely proportional to gate area!
Small-Signal Impedance:
Simple Current Source (Finite $r_o$)

$$r_{out} = \frac{1}{g_o}$$
Small-Signal Impedance: “Diode” Load (Finite $r_o$)

$$r_{out} = \frac{1}{g_m} \left| r_o = \frac{1}{g_m + g_o} \approx \frac{1}{g_m} \right.$$
Small-Signal Impedance:
Looking Into Source (Finite $r_o$ and $g_{mb}$)

\[ i_o = (g_m + g_{mb})v_o + \frac{v_o}{r_o} = (g_m + g_{mb} + g_o)v_o \]

\[ r_{out} = \frac{1}{g_m + g_{mb} + g_o} = \frac{1}{g_m} \parallel \frac{1}{r_o} \approx \frac{1}{g_m} \]
Small-Signal Impedance:
Looking Into Source w/ $R_D$ (Finite $r_o$ and $g_{mb}$)

$$r_{out} = \frac{1}{g_m + g_{mb} + g_o \left( 1 + \frac{R_D}{r_o} \right)}$$
Small signal analysis: Common-source amplifier

Small signal equivalent

If $V_{OUT} > V_{DSAT1}$, $V_{OUT} < V_{DD} - V_{SAT2}$

$A_v = -\frac{g_{m1}}{g_{01} + g_{02}}$

$g_{m1}, g_{01},$ and $g_{02}$ are function of $Q$
Small signal analysis: Common-drain (source follower) amplifier

Small signal equivalent circuit

\[
\frac{V_{out}}{V_{in}} = \frac{g_{ml}}{g_{ml} + g_{mb} + g_{01} + g_{02}}
\]

How this is done?
Why?
Small signal analysis: Common-gate amplifier (cascode)

\[ \frac{v_{out}}{v_{in}} = g_{m1} + g_{mb} + g_{01} \]

\[ g_{01} + g_{02} \]

Impedance seen at Vin and Vout? Are they relevant?
Precise Current Mirrors: Cascode structure

Error \approx \lambda_2 V_{DS2} - \lambda_1 V_{DS1}

FUNDAMENTAL PRINCIPLE:

Error can be reduced if and only \lambda_2=\lambda_1 and V_{DS2}=V_{DS1}

\Rightarrow Transistors M1 and M2 are used as current mirrors

\Rightarrow Transistors M3 and M4 are used to have V_{DS1}=V_{DS2}

\Rightarrow L1=L2 and ID1=ID2 \Rightarrow \lambda_1=\lambda_2

\Rightarrow If M1=M2 then \mu_1=\mu_2, and VT1=VT2
MOS Cascode Topology

Writing a KCL at the output node:

\[ -i_o + g_{m3}(-v_x) + \frac{v_o - v_x}{r_{o3}} = 0 \]

\[ -i_o - g_{m3}i_o r_{o1} - \frac{i_o r_{o1}}{r_{o3}} = -\frac{v_o}{r_{o3}} \]

The dominant term is the bottom effective resistance boosted by the gain of the top transistor \((g_{m3} r_{o3})\)
Comparison of current sources: output impedance and headroom

\[ r_{\text{out}} = r_{02} \]

\[ V_0 > V_{\text{DSAT2}} \]

\[ V_0 > V_{\text{GS1}} + V_{\text{DSAT4}} = V_{\text{T1}} + V_{\text{DSAT1}} + V_{\text{DSAT4}} \]

\(~100-400\, \text{mV}\)

\(~0.9-1.5\, \text{V!}\)
Double Cascode Structure: Advantages and drawbacks!

Small signal output resistance:

\[ r_{out} \approx g_{m4}(r_{eq31})r_{04} \approx g_{m4}(g_{m3}r_{02}r_{03})r_{04} \]

\[ V_0 > V_{DS2} + V_{DSAT3} + V_{DSAT4} \]

Output resistance is increased

Voltage swing is reduced

Parasitic poles could be an issue

How VG3 and VG4 can be generated????

Usually this section is more complex to ensure VDS is similar in both transistors M1 and M2
Voltage references (biasing cascode structures)

For minimum output Compliance voltage
Let's consider the case: \( V_{DS2} = V_{DSAT2} \)

\[ V_{GSR} = V_{TR} + \frac{2L_R}{\mu_nC_{OX}W_R}I_{D1} \]

Increasing \( L/W \) by 4, \( V_{DSAT} \) increases by 2

According to \( (W/L)_1 \), the gate dimensions for MR \( (W/L)_R \) must be designed

Problem: \( V_{TR} \neq VT3 \) due to body effect
Partial solution: \( (W/L)_1 > 4(W/L)_R \Rightarrow 9(W/L)_R \)

The accuracy will be somewhat off because \( V_{DS1} \neq V_{DS2} \)
Improved (self regulated) current source

What if we want route similar to a double cascode structure without the headroom cost?

\[ r_{out} \approx g_{m4} \left(1 + A_{V}\right)r_{02}r_{04} \]

Similar to double cascode
Other current sources

\[ i_D = \mu C_{OX} \frac{W}{L_{\text{eff}}} \left[ V_{GS} - V_T - 0.5 V_{DS} \right] V_{DS} \]

\[ r_{ds3} = \frac{L_{\text{eff}}}{\mu C_{OX} W \left[ V_{GS3} - V_T - V_{DS3} \right]} \]

\[ r_{out} \approx g_m \cdot 4 \cdot r_{04} \left( r_{ds3} \right) \]

\[ V_0 > V_{DS3} + V_{DSAT 4} \]

\[ r_{out} \approx g_m \cdot 4 \cdot r_{04} \left( \sum r_{dsi} \right) \]
Low-Voltage Cascode Current Mirror

- M2 and M4 should be sized such that
  - $V_{GS2} = V_{GS4}$
- M1 and M3 biased near edge of saturation
  - $V_{DS1} \approx V_{DS3} \approx V_{DSAT}$
  - $V_b = V_{GS2} + (V_{GS1} - V_{T1}) = V_{GS4} + (V_{GS3} - V_{T3})$
- Alternative $V_b$ generation circuit
  - M5 sized such that $V_{GS5} \approx V_{GS2}$
    - Some body effect error here
  - Size M6 and Rb such that
    - $V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{T1}$
Next Time

- Single-Stage Amplifiers