ECEN474/704: (Analog) VLSI Circuit Design
Spring 2018

Lecture 9: Differential Amplifiers

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Announcements & Agenda

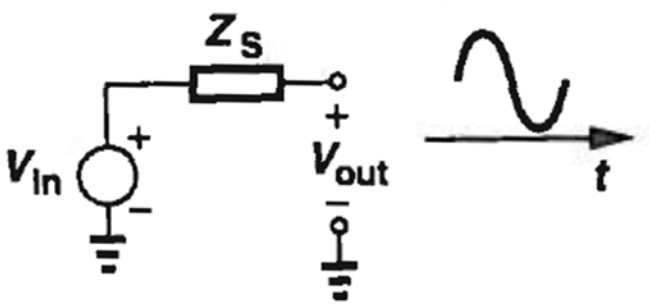
- HW2 Due Mar 6
- Reading
  - Razavi Chapter 4

- Single-ended and differential signals
- Differential pair
- Differential amplifiers

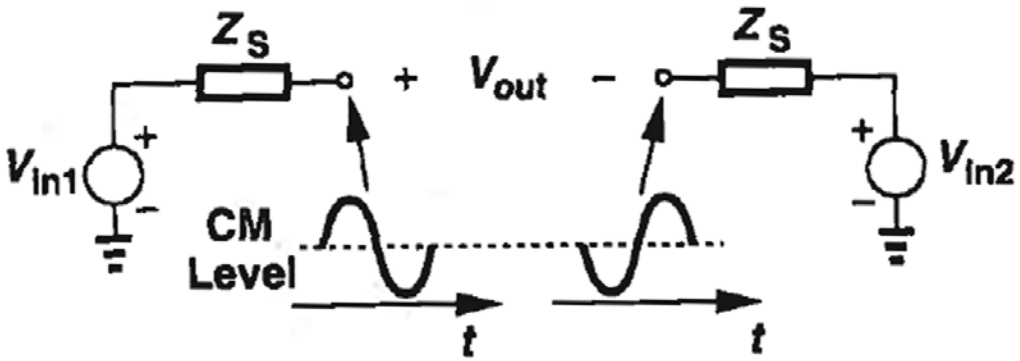
Single-Ended & Differential Signals

- A single-ended signal is measured with respect to a fixed potential (ground)
- A differential signal is measured between two equal and opposite signals which swing around a fixed potential (common-mode level)
- You can decompose differential signals into a differential mode (difference) and a common-mode (average

Single-Ended Signal



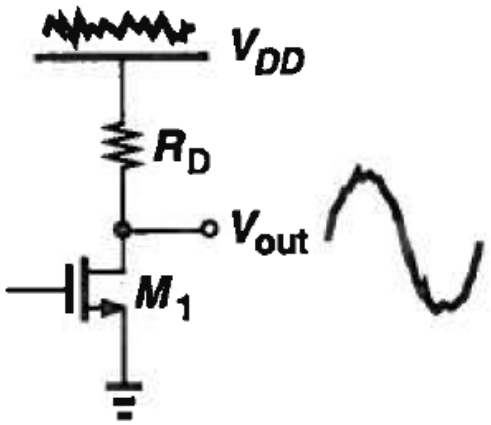
Differential Signal



$$V_{DM} = V_{out}^{+} - V_{out}^{-} \qquad V_{CM} = \frac{V_{out}^{+} + V_{out}^{-}}{2}$$

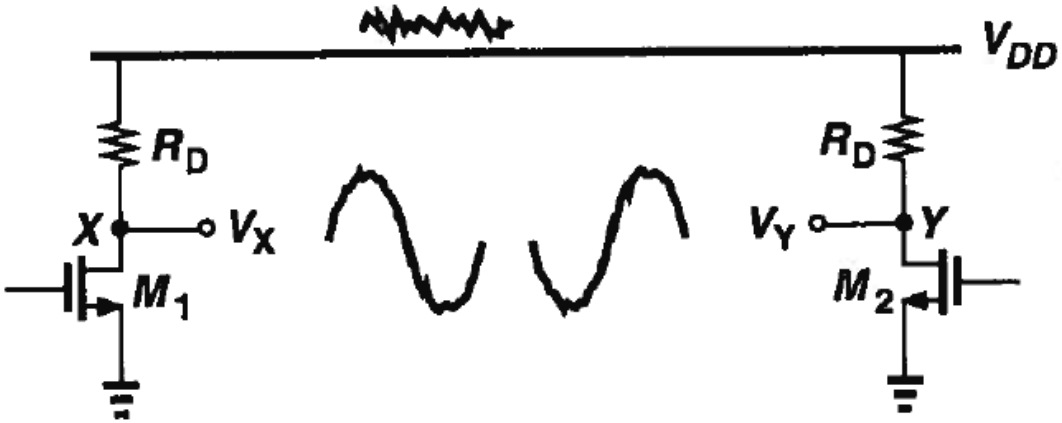
Single-Ended & Differential Amplifiers

- Differential signaling advantages
  - Common-mode noise rejection
  - Higher (ideally double) potential output swing
  - Simpler biasing
  - Improved linearity
- Main disadvantage is area, which is roughly double
  - Although, to get the same performance in single-ended designs, we often have to increase the area dramatically



Max Output Swing

$$V_{DD} - (V_{GS} - V_{Tn})$$

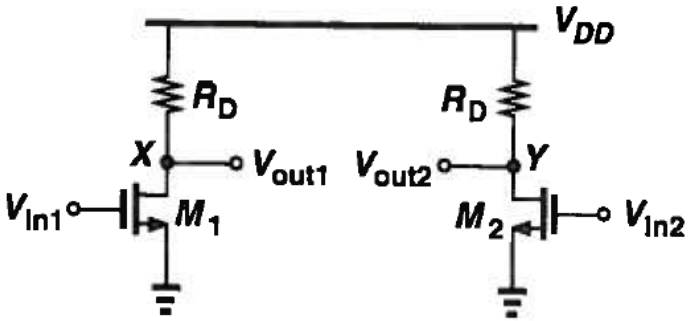


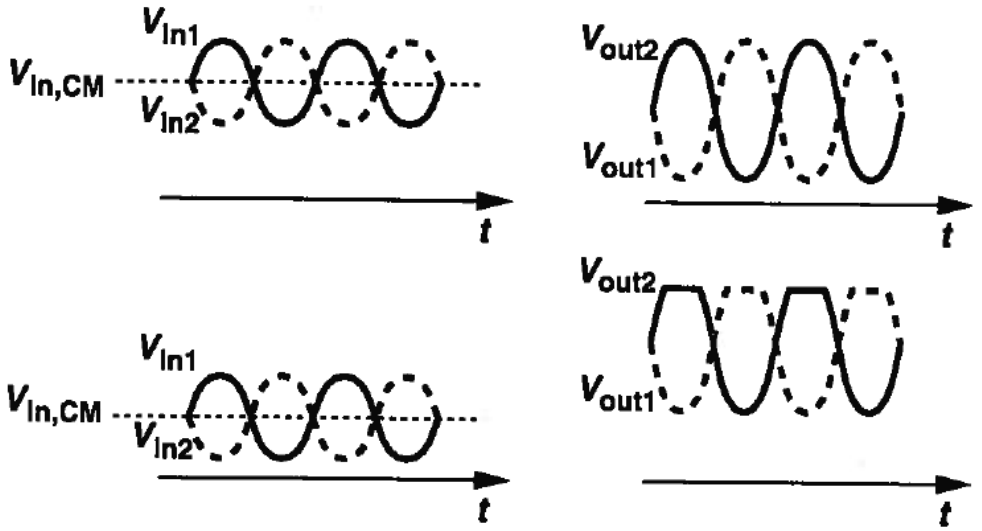
Max Output Swing

$$2(V_{DD} - (V_{GS} - V_{Tn}))$$

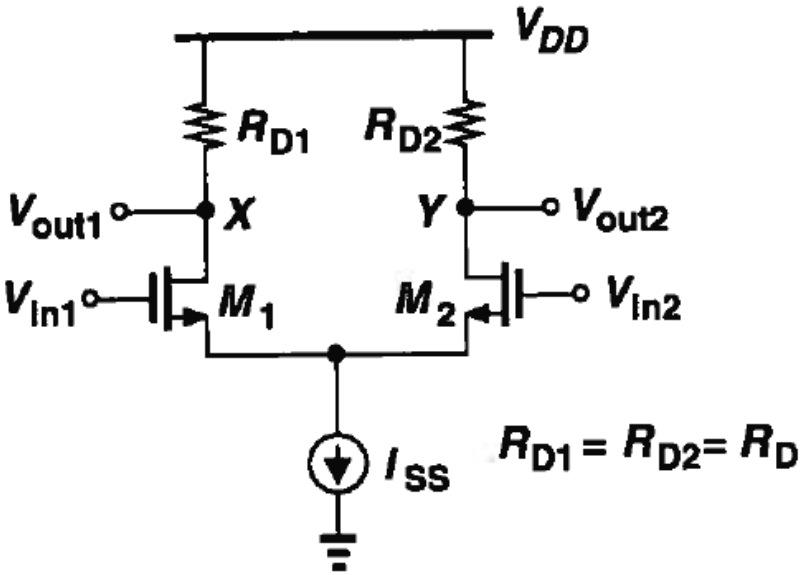
Common-Mode Level Sensitivity

- A design which uses two single-ended amplifiers to realize a differential amplifier is very sensitive to the common-mode input level
- The transistors' bias current and transconductance can vary dramatically with the common-mode input
  - Impacts small-signal gain
  - Changes the output common-mode, which impacts the maximum output swing





Differential Pair



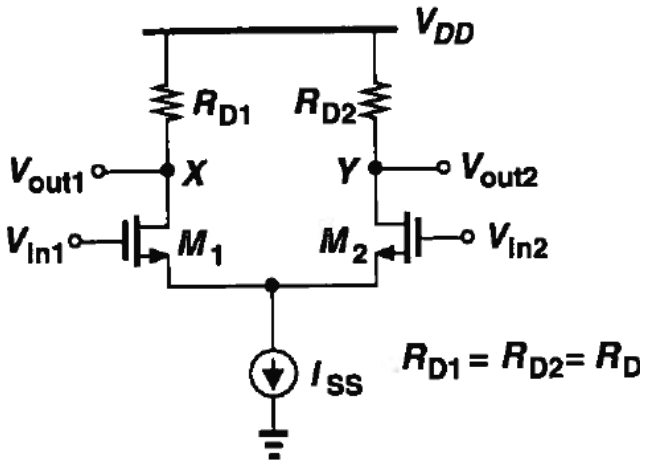
$$A_{DM} = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} = -g_m R_D$$

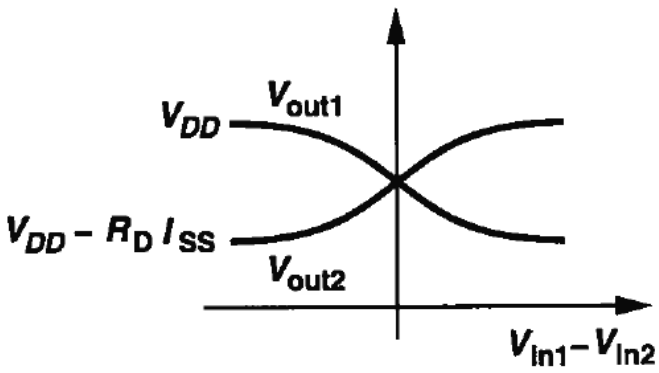
where $g_m = g_{m1} = g_{m2}$ and $R_D = R_{D1} = R_{D2}$

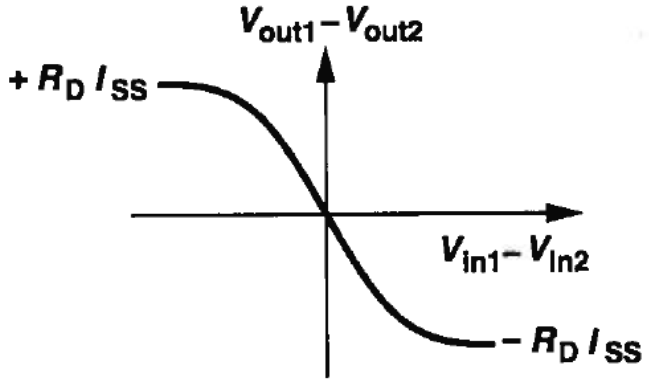
$$V_{O,CM} = V_{DD} - \left(\frac{I_{SS}}{2}\right) R_D$$

- An improved differential amplifier topology utilizes a “tail” current source to keep the transistor bias current ideally constant over the common-mode input range
- Allows for a constant small-signal gain and output common-mode level
  - Note, you still have to have keep the input pair and tail current source transistors in saturation

Differential Pair Input-Output Characteristics



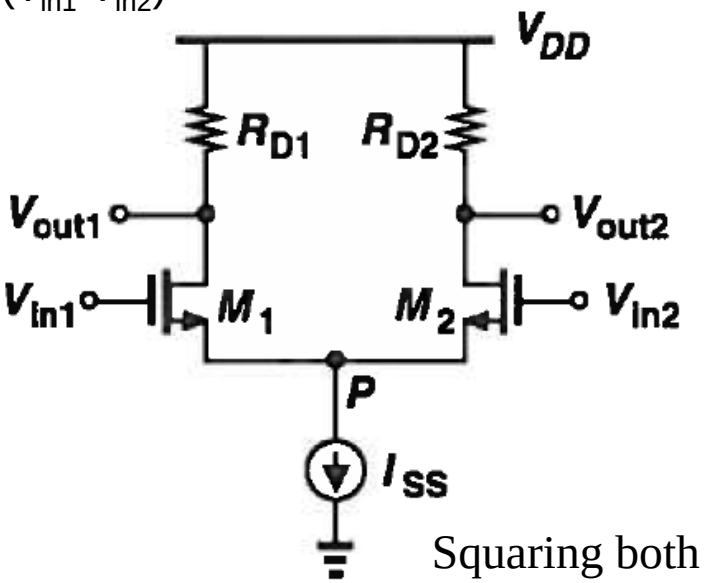




- For large-signal differential inputs, the maximum output levels are well defined and ideally independent of the input common-mode
- For small-signal differential inputs, the small-signal gain is maximum at low-input signal levels
  - As the differential input level increases, the circuit becomes more nonlinear and the gain decreases

Differential Pair I-V Characteristics (Large Signal)

Objective: Find the differential transistor current (I_{D1}-I_{D2}) as a function of the input differential voltage (V_{in1}-V_{in2})



Input Voltage Difference: $V_{in1} - V_{in2} = V_{GS1} - V_{GS2} = (V_{GS1} - V_T) - (V_{GS2} - V_T)$

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

Squaring both sides and using $I_{D1} + I_{D2} = I_{SS}$

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{SS} - 2\sqrt{I_{D1}I_{D2}}\right)$$

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}$$

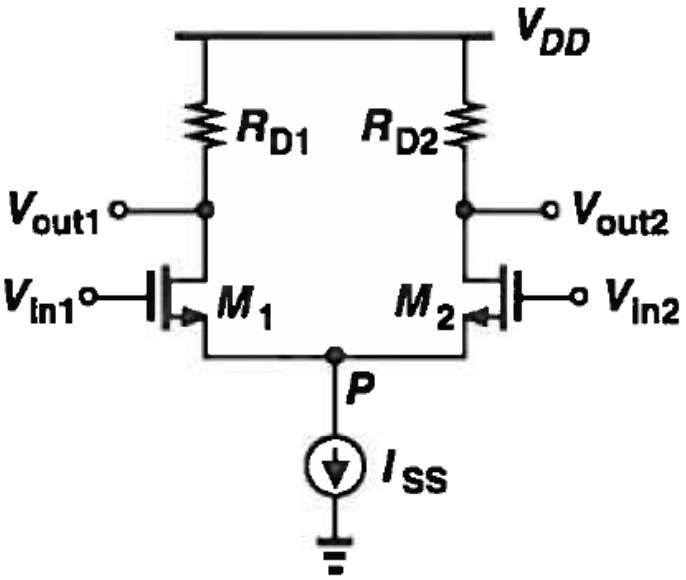
Squaring both sides and using $4I_{D1}I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I_{ss}^2 - (I_{D1} - I_{D2})^2$

$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

*Note, this equation is only valid for a certain maximum input differential voltage (V_{in1}-V_{in2})

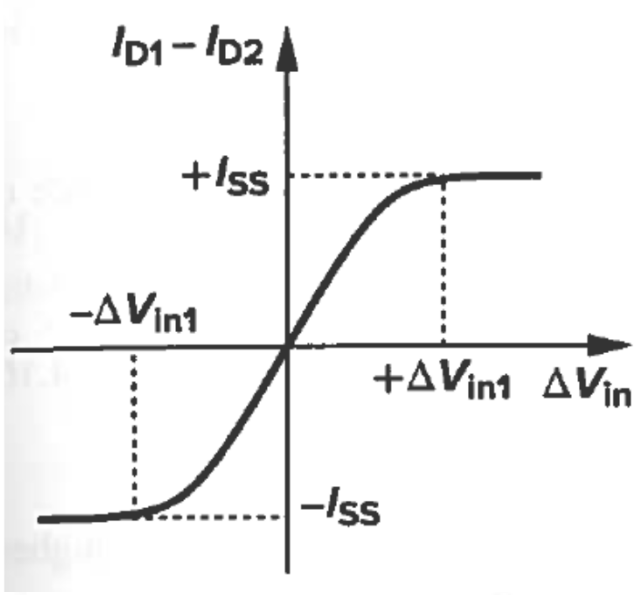
$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

Differential Pair I-V Characteristics (Large Signal)

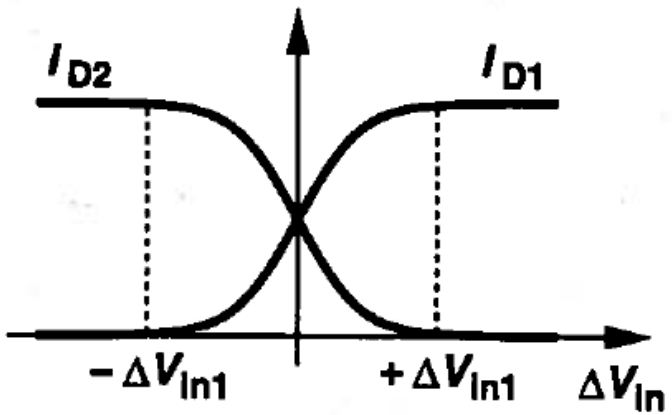


$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$\Delta V_{in1} = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox}\frac{W}{L}}}$$



- The differential current is an odd function of the differential input voltage which increases linearly for small inputs
- For large differential input voltages, the output differential current compresses due to the sqrt term
- The differential output current maxes out when all the current flows through one transistor at ΔV_{in1}



Differential Pair I-V Characteristics (Large Signal)

For the maximum current range consider the case when all current flows through M1

$$I_{D1} - I_{D2} = I_{D1} - 0 = I_{SS} \Rightarrow I_{D1} = I_{SS}$$

For $I_{D2} = 0$, ideally $V_{GS2} = V_T$

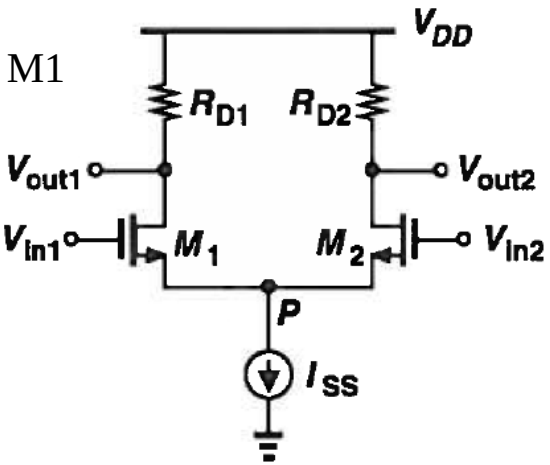
$$\Delta V_{in} = V_{GS1} - V_{GS2} = V_{GS1} - V_T = \Delta V_{in1}$$

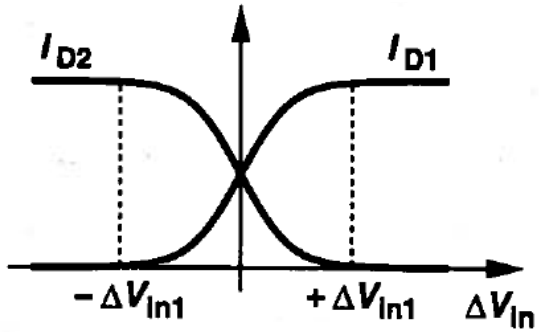
At this ΔV_{in1}, M1 must support all of I_{SS}

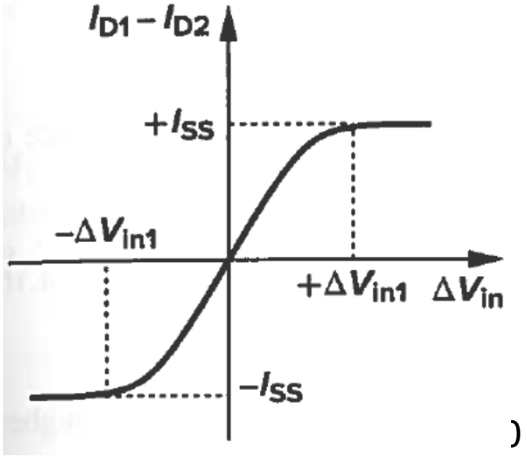
Maximum Differential Input : $\Delta V_{in1} = V_{GS1} - V_T = \sqrt{\dfrac{2I_{SS}}{\mu_n C_{ox} \dfrac{W}{L}}}$

We can relate this to the zero differential input overdrive

Zero Differential Input Overdrive : $(V_{GS} - V_T)_{1,2} = \sqrt{\dfrac{I_{SS}}{\mu_n C_{ox} \dfrac{W}{L}}} = \dfrac{\Delta V_{in1}}{\sqrt{2}}$







- The differential output current will saturate if the differential input voltage exceeds sqrt(2) times the equilibrium input overdrive voltage

Differential Pair Transconductance

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

Define $\Delta I_D = I_{D1} - I_{D2}$ and $\Delta V_{in} = V_{in1} - V_{in2}$

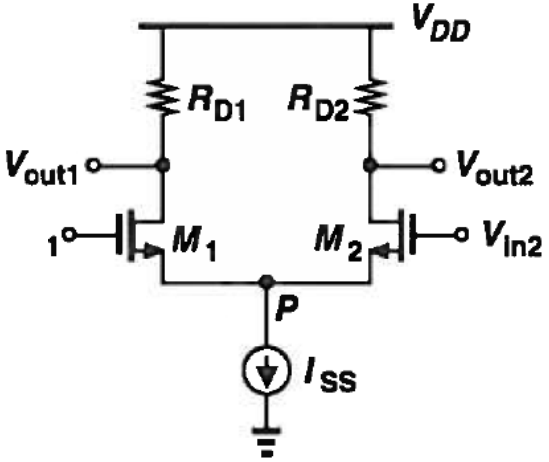
$$G_m = \frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

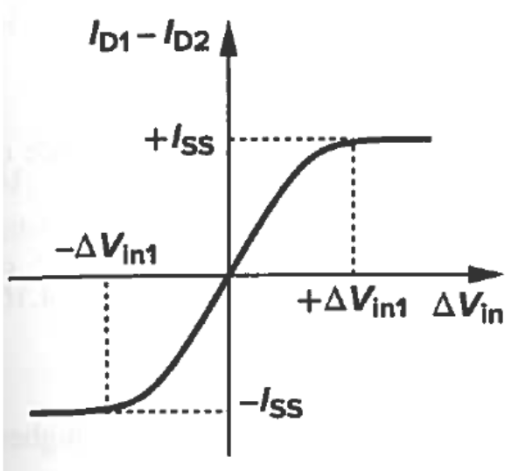
The small-signal transconductance at $\Delta V_{in} = 0$ is

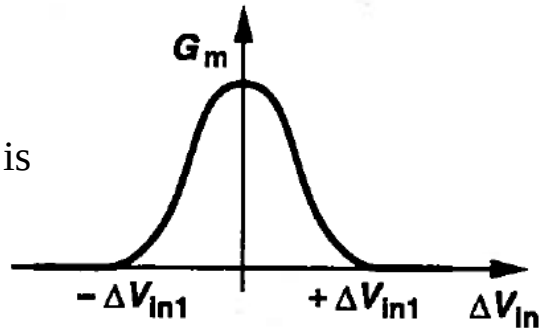
$$G_m = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{ss}}$$

Considering the load resistors R_D, the small-signal gain is

$$|A_v| = G_m R_D = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{ss}}\, R_D$$

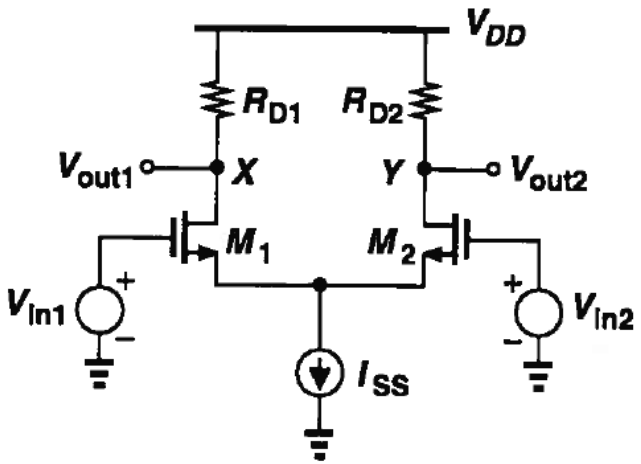




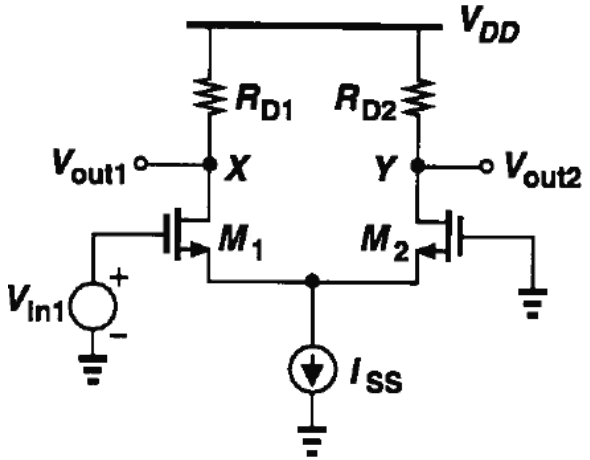


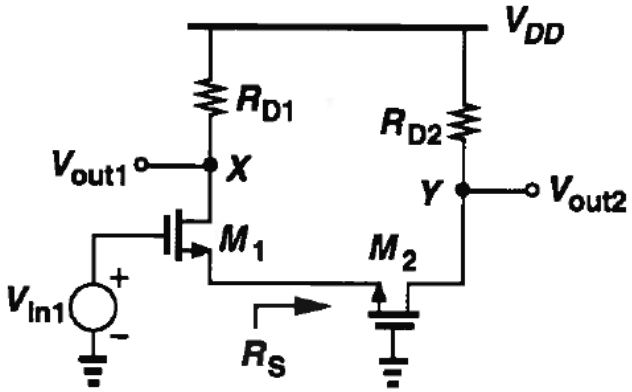
- The differential pair transconductance and gain is maximum near zero input differential voltage

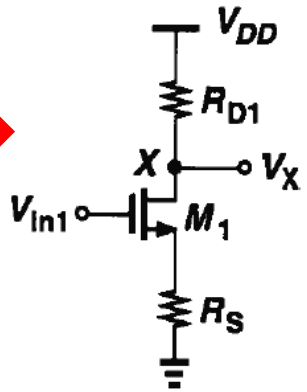
Differential Pair Small-Signal Analysis Method 1 - Superposition



Find $V_{out}(V_{in1})$





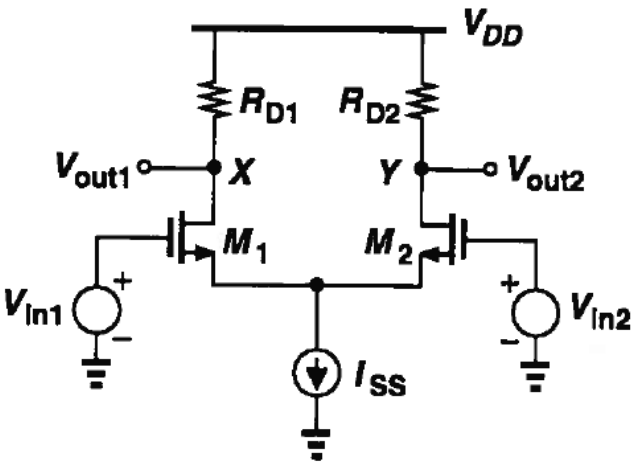


Note that $g_{m1} = g_{m2} = g_m$ and $R_{D1} = R_{D2} = R_D$

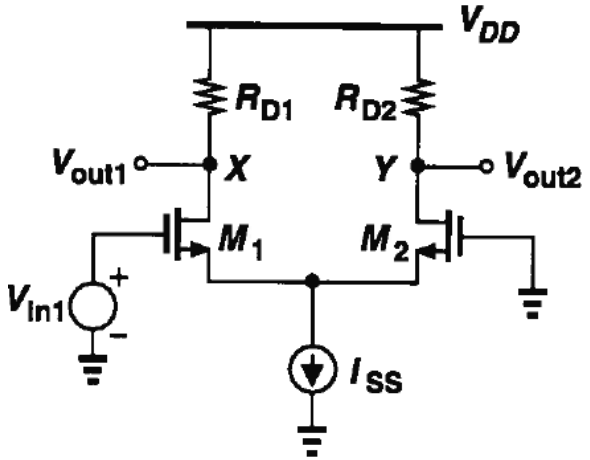
$$\frac{V_X}{V_{in1}} = \frac{-g_{m1}R_{D1}}{1+\frac{g_{m1}}{g_{m2}}} = -\frac{g_m R_D}{2}$$

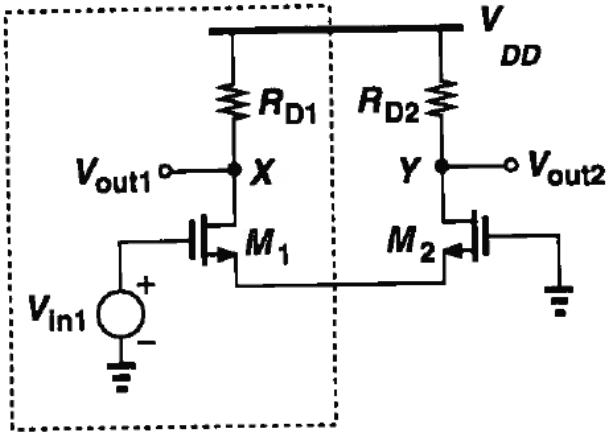
- The X output from Vin1 is modeled as a degenerated CS amplifier

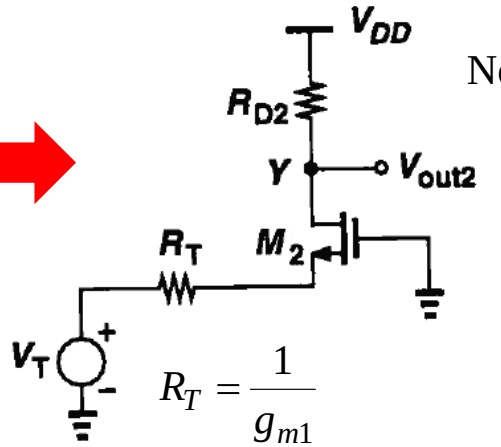
Differential Pair Small-Signal Analysis Method 1 - Superposition



Find $V_{out}(V_{in1})$





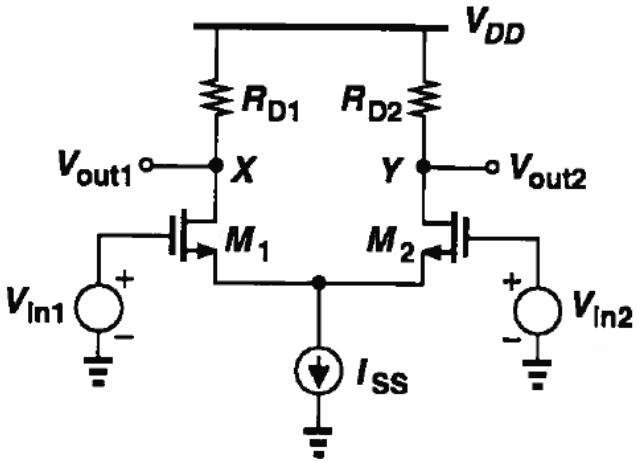


Note that $g_{m1} = g_{m2} = g_m$ and $R_{D1} = R_{D2} = R_D$

$$\frac{V_Y}{V_{in1}} = \frac{g_{m2}R_{D1}}{1+\frac{g_{m2}}{g_{m1}}} = \frac{g_m R_D}{2}$$

- The Y output from Vin1 is modeled as a Thevenin equivalent driving a CG amplifier

Differential Pair Small-Signal Analysis Method 1 - Superposition



To find the total $V_{out}\big|_{V_{in1}}$

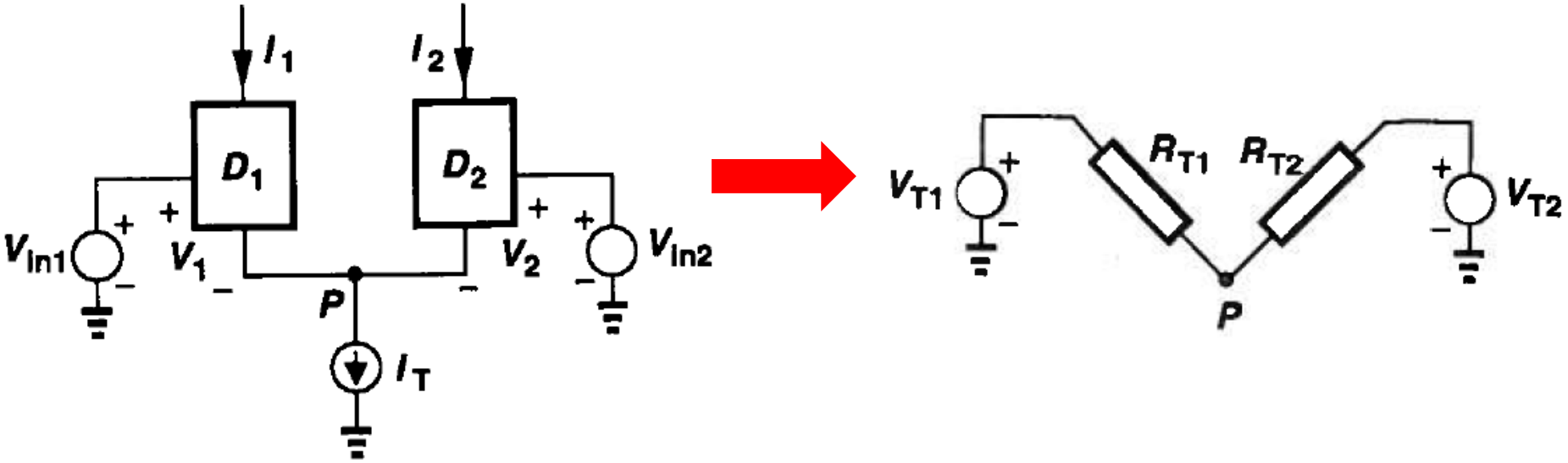
$$V_{out}\big|_{V_{in1}} = (V_X - V_Y)\big|_{V_{in1}} = \left(\frac{-g_{m1}R_{D1}}{1+\frac{g_{m1}}{g_{m2}}} - \frac{g_{m2}R_{D1}}{1+\frac{g_{m2}}{g_{m1}}} \right) V_{in1} = \left(\frac{-g_m R_D}{2} - \frac{g_m R_D}{2} \right) V_{in1} = -g_m R_D V_{in1}$$

From the circuit symmetry, $V_{out}\big|_{V_{in2}} = -V_{out}\big|_{V_{in1}}$

$$V_{out}\big|_{V_{in2}} = (V_X - V_Y)\big|_{V_{in2}} = g_m R_D V_{in2}$$

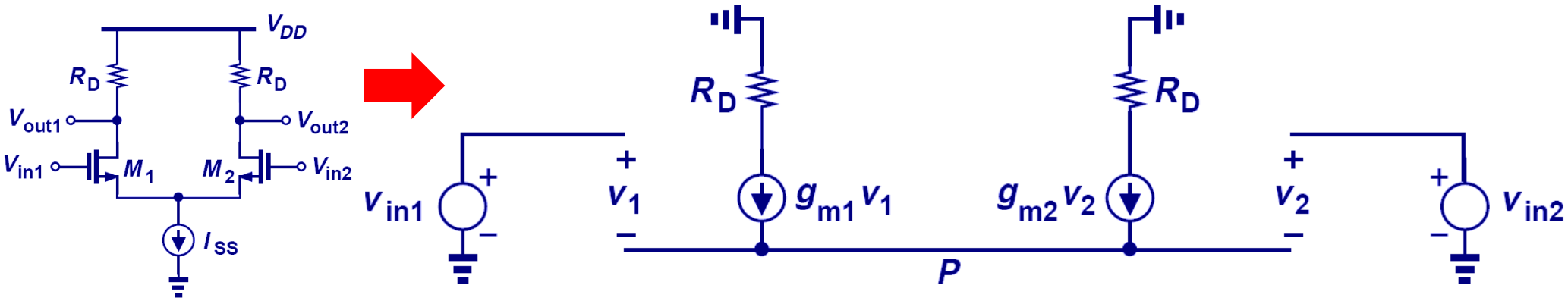
$$\text{Differential Gain}: \frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = \frac{-g_m R_D (V_{in1} - V_{in2})}{V_{in1} - V_{in2}} = -g_m R_D$$

Differential Pair Small-Signal Analysis Method 2 – Half Circuit



- The symmetric differential pair can be modeled as a Thevenin equivalent to observe how the tail node P changes with the differential input signal
- If $R_{T1}=R_{T2}$ and the input is a truly differential signal, node P remains constant
- This allows the tail node to be treated as a “virtual ground”

Virtual GND Proof



1. KVL around the input networks

$$v_{in1} - v_1 = v_P = v_{in2} - v_2$$

2. KCL at node P

$$g_{m1}v_1 + g_{m2}v_2 = 0$$

For small signals $g_{m1} = g_{m2}$

$$v_1 = -v_2$$

For differential operation $v_{in1} = -v_{in2}$, and using the above KVL

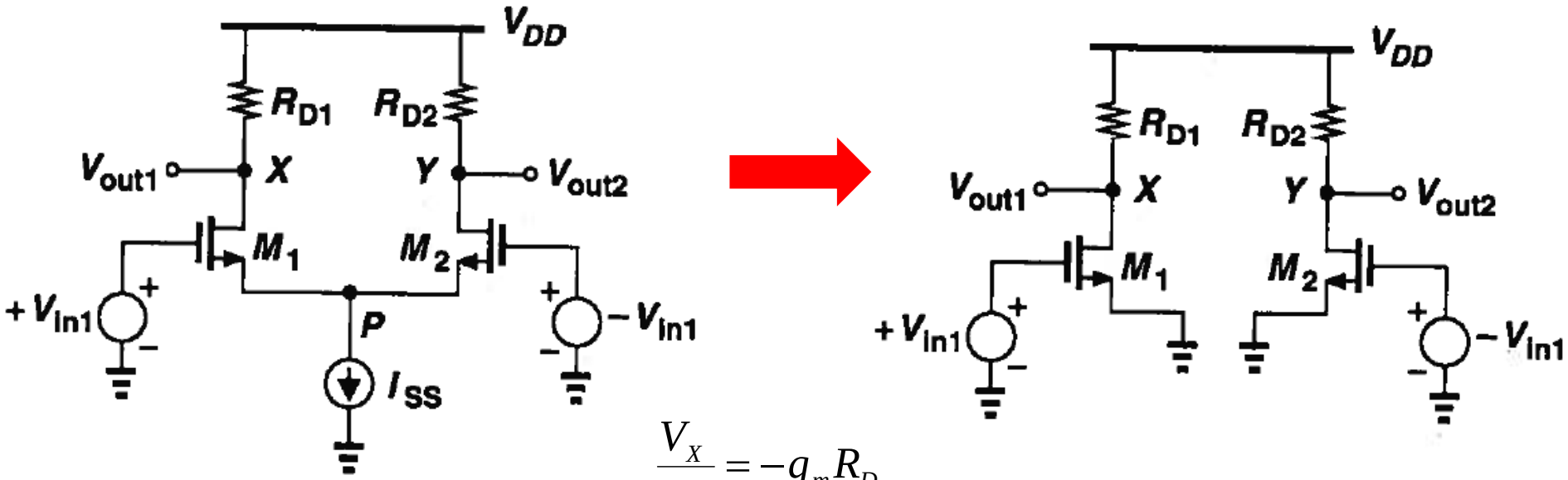
$$2v_{in1} = 2v_1$$

which implies that

$$v_P = v_{in1} - v_1 = 0$$

Differential Pair Small-Signal Analysis Method 2 – Half Circuit

- Applying the virtual ground concept allows modeling as two “half circuits”



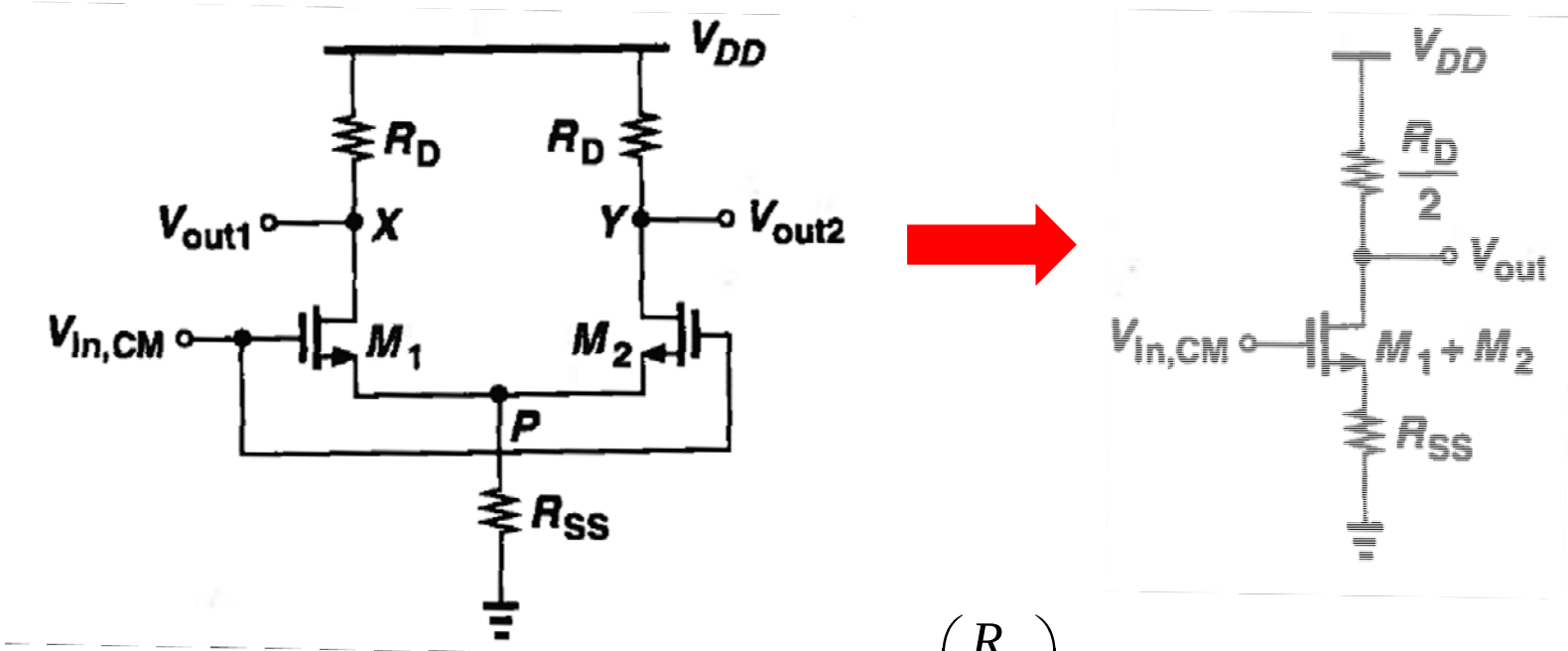
$$\frac{V_X}{V_{in1}} = -g_m R_D$$

$$\frac{V_Y}{(-V_{in1})} = -g_m R_D$$

$$\text{Differential Gain}: \quad \frac{V_X - V_Y}{V_{in1} - (-V_{in1})} = -\frac{2g_m R_D V_{in1}}{2V_{in1}} = -g_m R_D$$

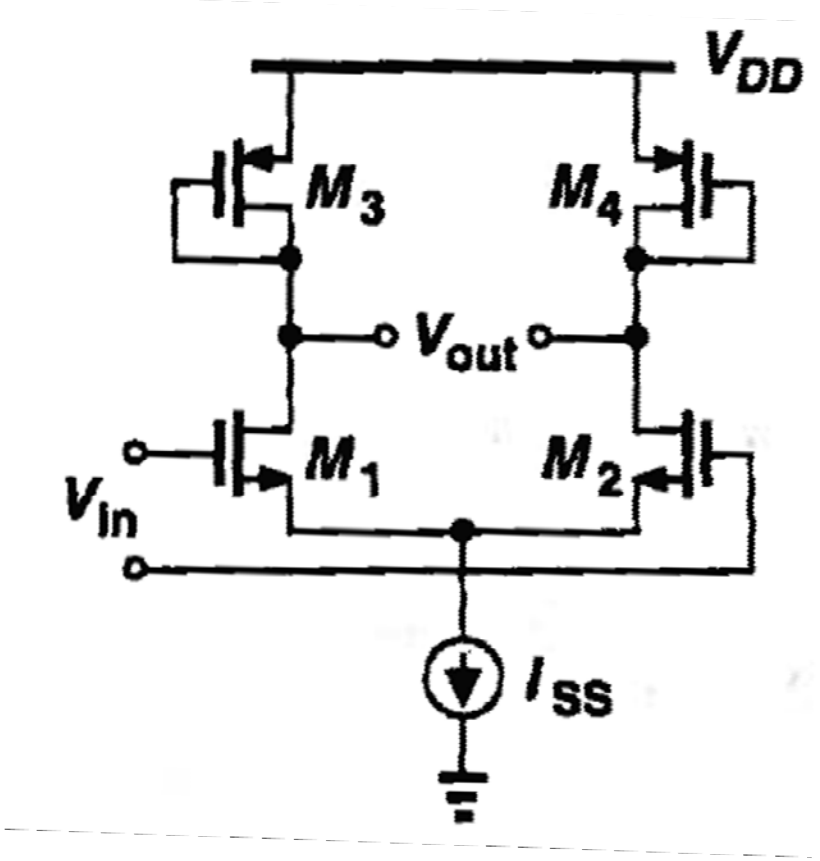
Differential Pair Common-Mode Response

- Ideally, a differential amplifier completely rejects common-mode signals, i.e. $A_{v,CM}=0$
- In reality, the finite tail current source impedance results in a finite common-mode gain



$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = -\frac{2g_m\left(\frac{R_D}{2}\right)}{1+2g_mR_{SS}} = -\frac{g_mR_D}{1+2g_mR_{SS}}$$

Differential Pair with Diode Loads



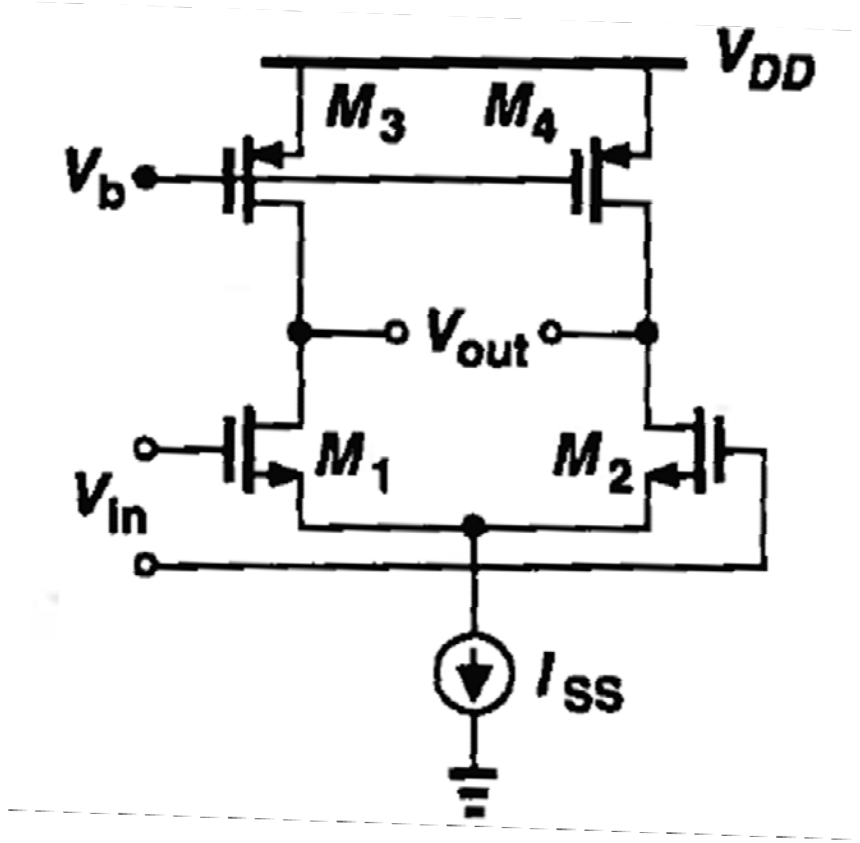
Assuming $\gamma = 0$

$$A_v = -\frac{g_{m1}}{g_{o1} + g_{m3} + g_{o3}} \approx -\frac{g_{m1}}{g_{m3}}$$

$$A_v \approx -\frac{g_{m1}}{g_{m3}} = -\frac{\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{SS}}}{\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_3 I_{SS}}} = -\sqrt{\frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_3}}$$

- While the gain of this amplifier is relatively small, it is somewhat predictable, as it is defined by the ratio of the transistor sizes and the n/p mobility

Differential Pair w/ Current-Source Loads

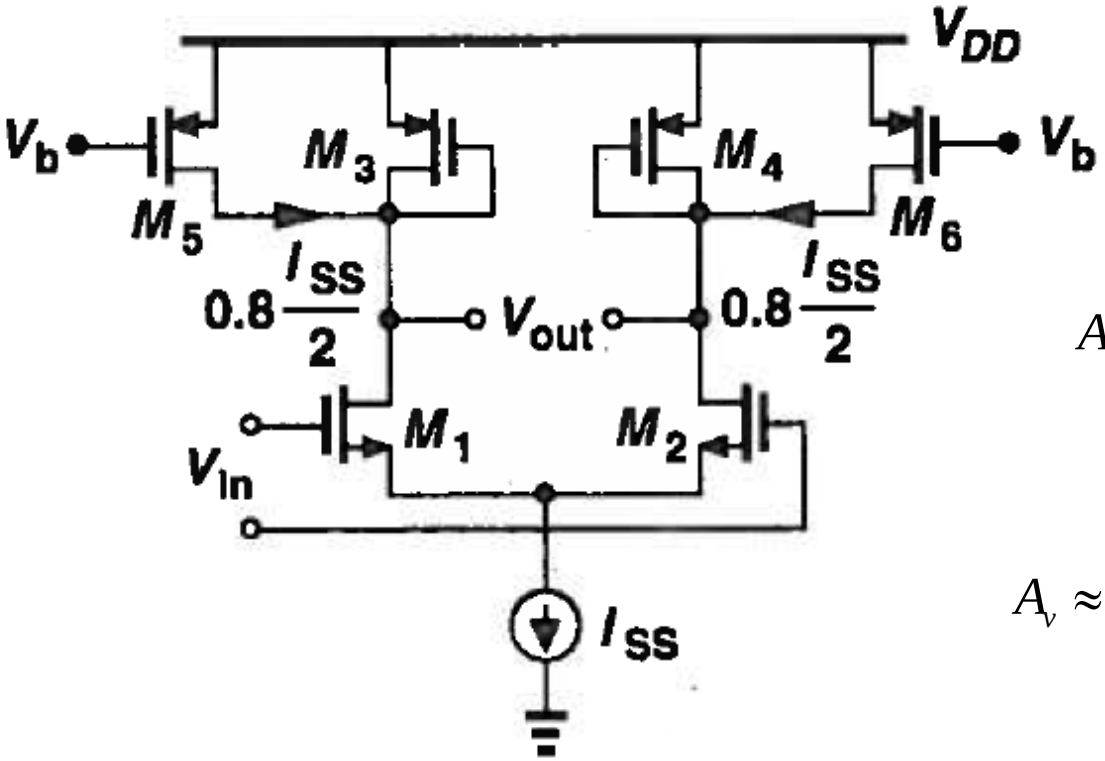


Assuming $\gamma = 0$

$$A_v = -\frac{g_{m1}}{g_{o1} + g_{o3}}$$

- While the gain of this amplifier is higher, it is somewhat unpredictable, as it is defined by the transistor output resistance, which changes dramatically with process variations

Differential Pair w/ Diode & Parallel Current-Source Loads



Assuming $\gamma = 0$

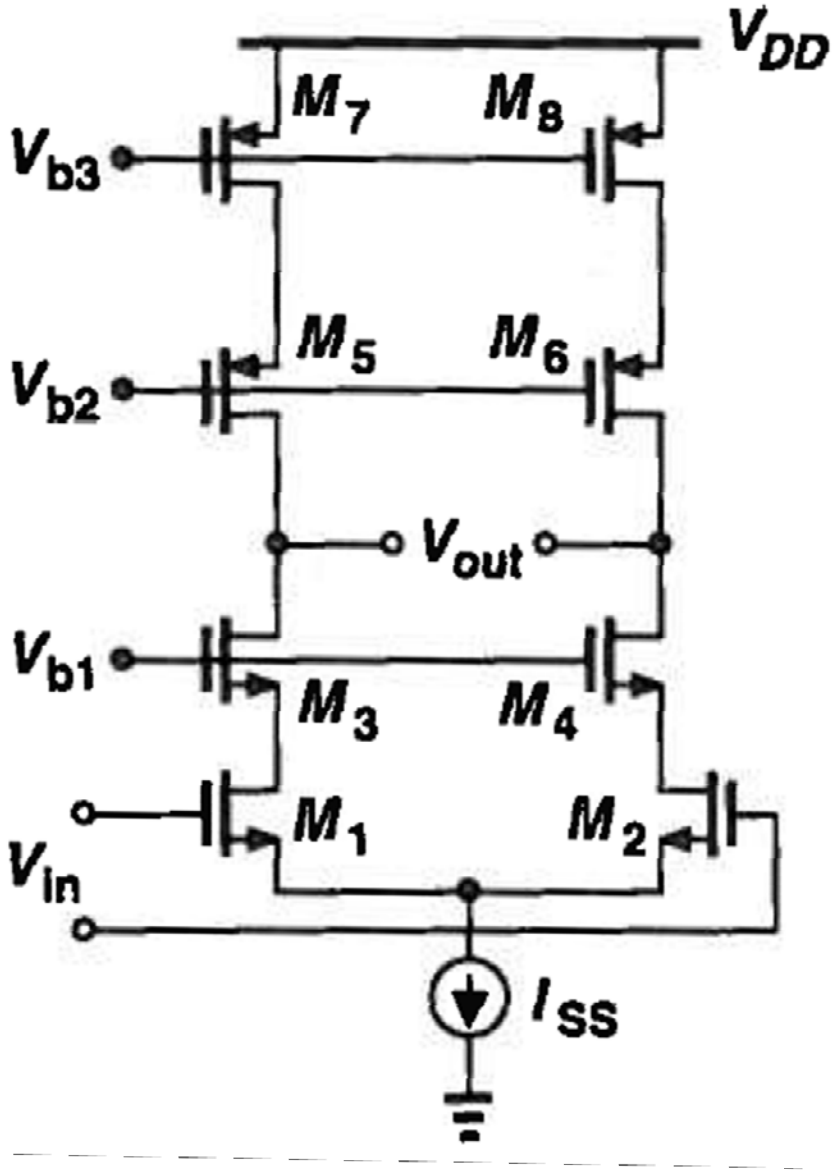
$$A_v = -\frac{g_{m1}}{g_{o1} + g_{m3} + g_{o3} + g_{o5}} \approx -\frac{g_{m1}}{g_{m3}}$$

$$A_v \approx -\frac{g_{m1}}{g_{m3}} = -\frac{\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{SS}}}{\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_3 (1-\alpha) I_{SS}}}$$

where α is the current percentage that the current source "steals" from the diode load

- Adding a parallel current source to a diode connected load allows for increase gain which is still somewhat predictable

Cascode Differential Pair



Assuming $\gamma = 0$

$$A_v = -g_{m1}\left(\left(r_{o3} + r_{o1} + g_{m3}r_{o1}r_{o3}\right)\left\|\left(r_{o5} + r_{o7} + g_{m5}r_{o7}r_{o5}\right)\right.\right)$$

$$A_v \approx -g_{m1}\left(g_{m3}r_{o1}r_{o3}\left\|g_{m5}r_{o7}r_{o5}\right.\right)$$

- Using a cascode differential pair and cascode current-source loads allows for a considerable increase in gain
- However, a relatively large power supply may be required to supply the necessary voltage "headroom" to keep all the transistors in saturation

Next Time

- Simple OTA