

ECEN474/704: (Analog) VLSI Circuit Design Spring 2018

Lecture 13: Folded Cascode & Two Stage Miller OTA



Sam Palermo

Analog & Mixed-Signal Center

Texas A&M University

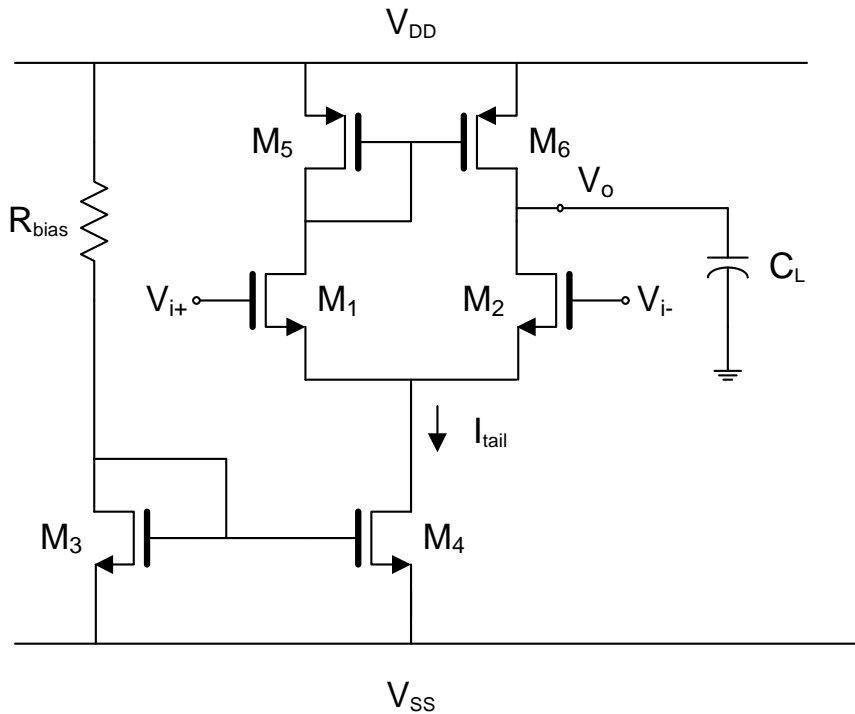
Announcements

- Exam dates reminder
 - Exam 2 is on Apr. 10
 - Exam 3 is on May 3 (3PM-5PM)
- Project description is posted on website

Agenda

- Single-Stage Cascode OTA
- Folded Cascode OTA
- Two Stage Miller OTA

Simple OTA

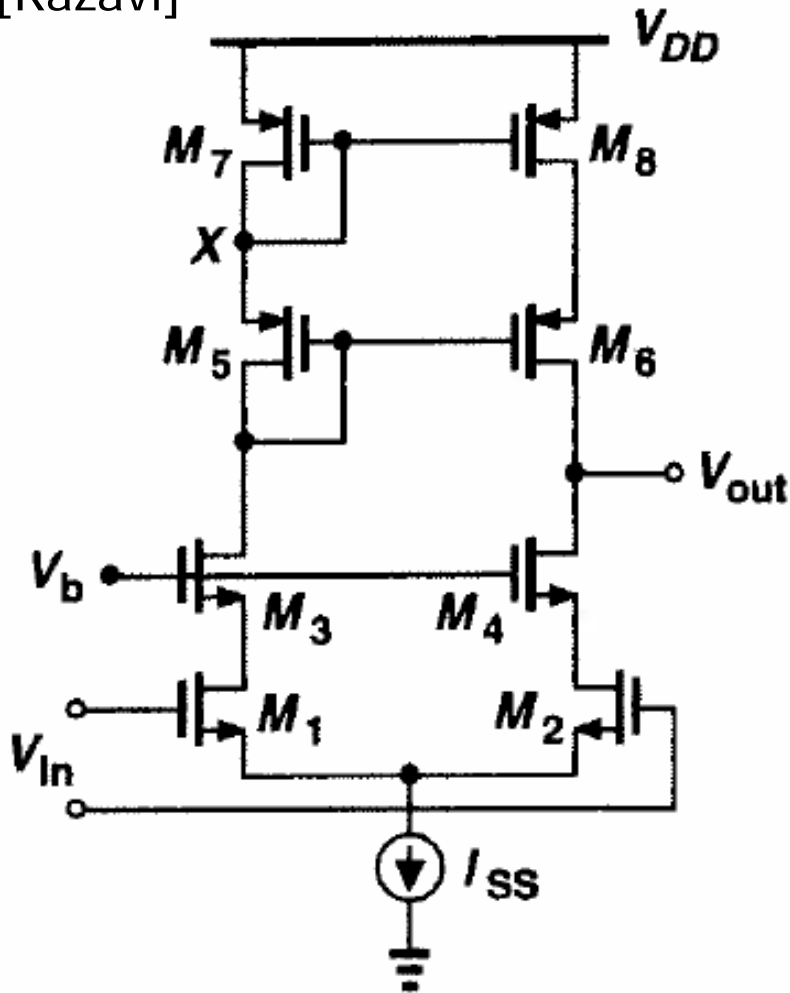


$$\text{DC Gain } A_v = G_m R_{out} = g_{m1} (r_{o2} \parallel r_{o6})$$

- Gain is limited by single-transistor output resistance

Single-Stage Cascode OTA

[Razavi]

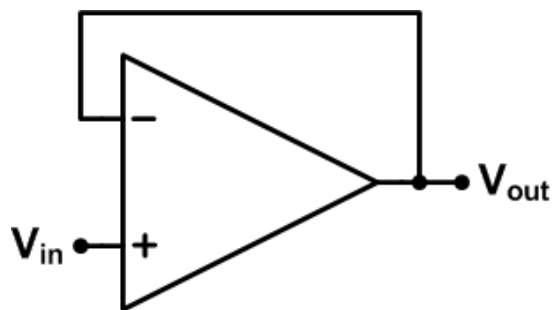


$$\text{DC Gain } A_v = G_m R_{out} \approx g_{m1} (g_{m4} r_{o2} r_{o4} \parallel g_{m6} r_{o8} r_{o6})$$

- Gain is larger by a $g_m r_o$ factor
- Output swing range is limited due to large compliance voltage of cascode current source load

Single-Stage Cascode OTA

Unity Gain Feedback Voltage Range



Minimum V_{out} set by M4 saturation

$$V_{out} \geq V_b - V_{TH4}$$

Maximum V_{out} set by M2 saturation

$$V_{out} \leq V_x + V_{TH2}$$

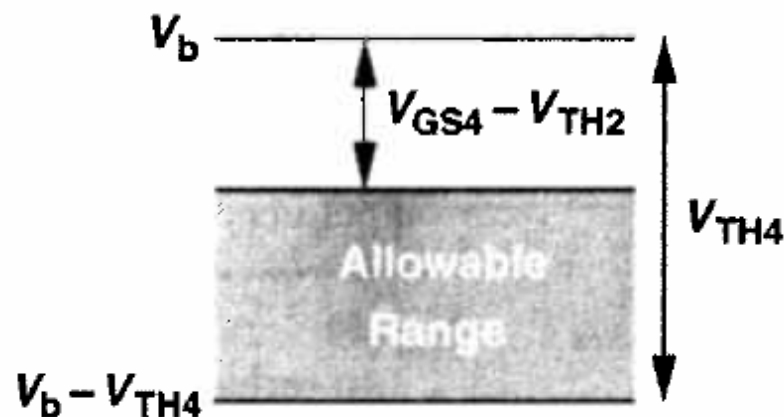
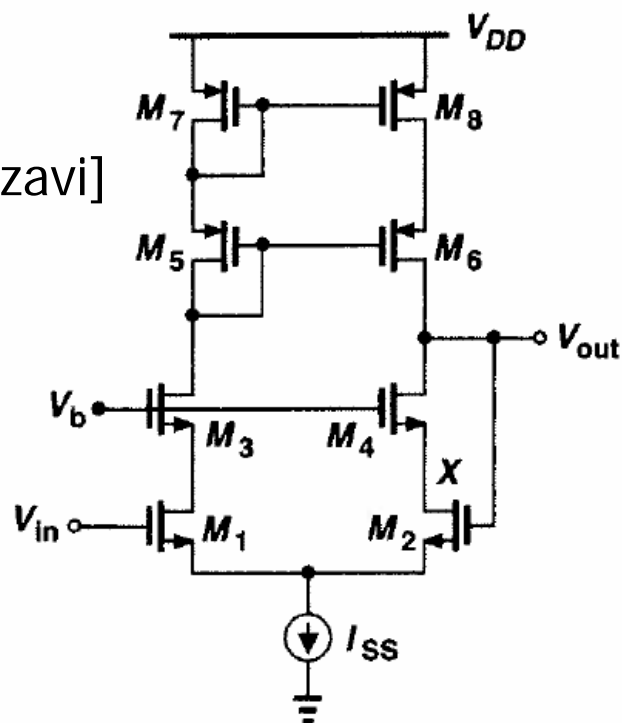
As $V_b = V_x + V_{GS4}$ and plugging V_x into M2 sat condition

$$V_{out} \leq V_x + V_{TH2} = V_b - V_{GS4} + V_{TH2} = V_b - (V_{GS4} - V_{TH2})$$

$$\text{Output (& Input) Range} = V_{TH4} - (V_{GS4} - V_{TH2})$$

Less than a V_{TH} !!!

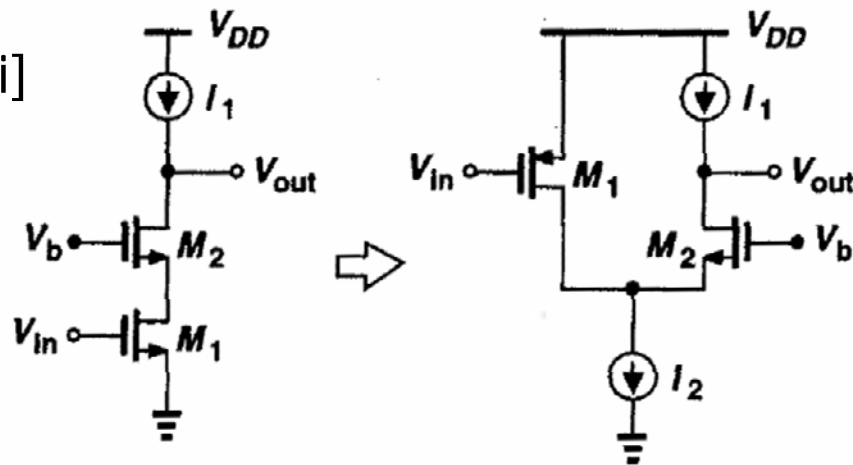
[Razavi]



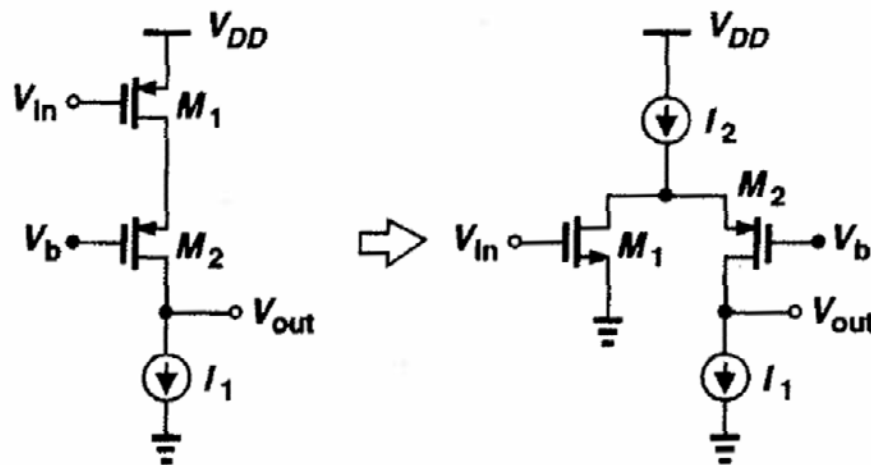
- Cascode configuration constrains output & unity-gain swing

Folded Cascode Circuits

[Razavi]



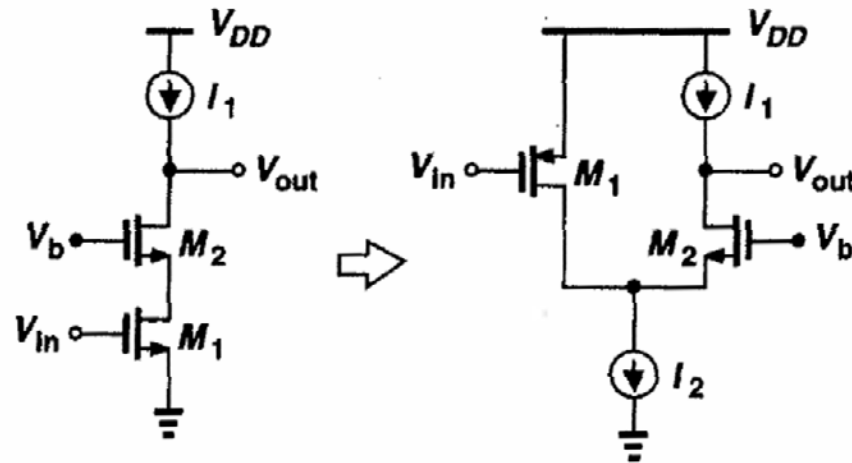
PMOS Input & NMOS Cascode



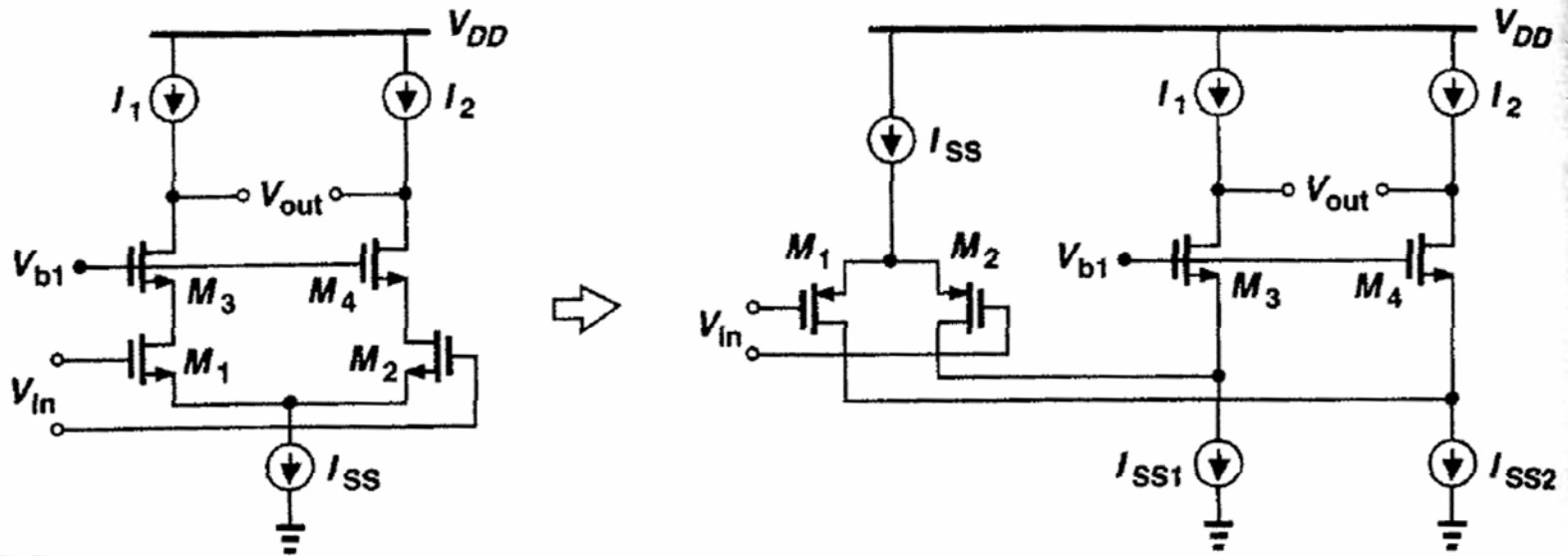
NMOS Input & PMOS Cascode

- “Folding” about the cascode node will increase input and output swing range

Folded Cascode OTA

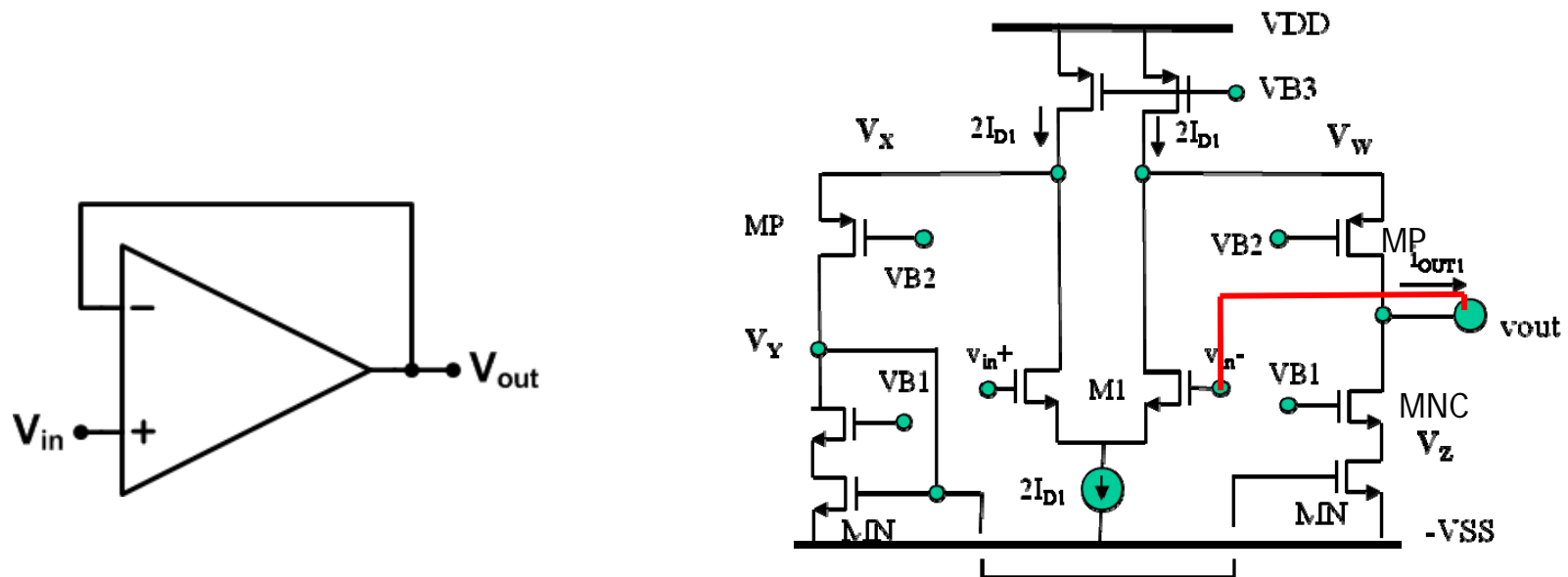


[Razavi]



Folded Cascode OTA

Unity Gain Feedback Voltage Range



Maximum V_{out} set by MP saturation

$$V_{out} \leq V_{b2} + |V_{THP}|$$

Minimum V_{out} set by output NMOS cascode or tail current source saturation

$$V_{out} \geq V_{DSATNC} + V_{DSATN} \quad \text{OR} \quad V_{out} \geq V_{DSATTail} + V_{GS1}$$

- With proper (high-value) choice of V_{b2} , a decent output and input swing range can be achieved

Folded-Cascode OTA: gm, rout and poles?

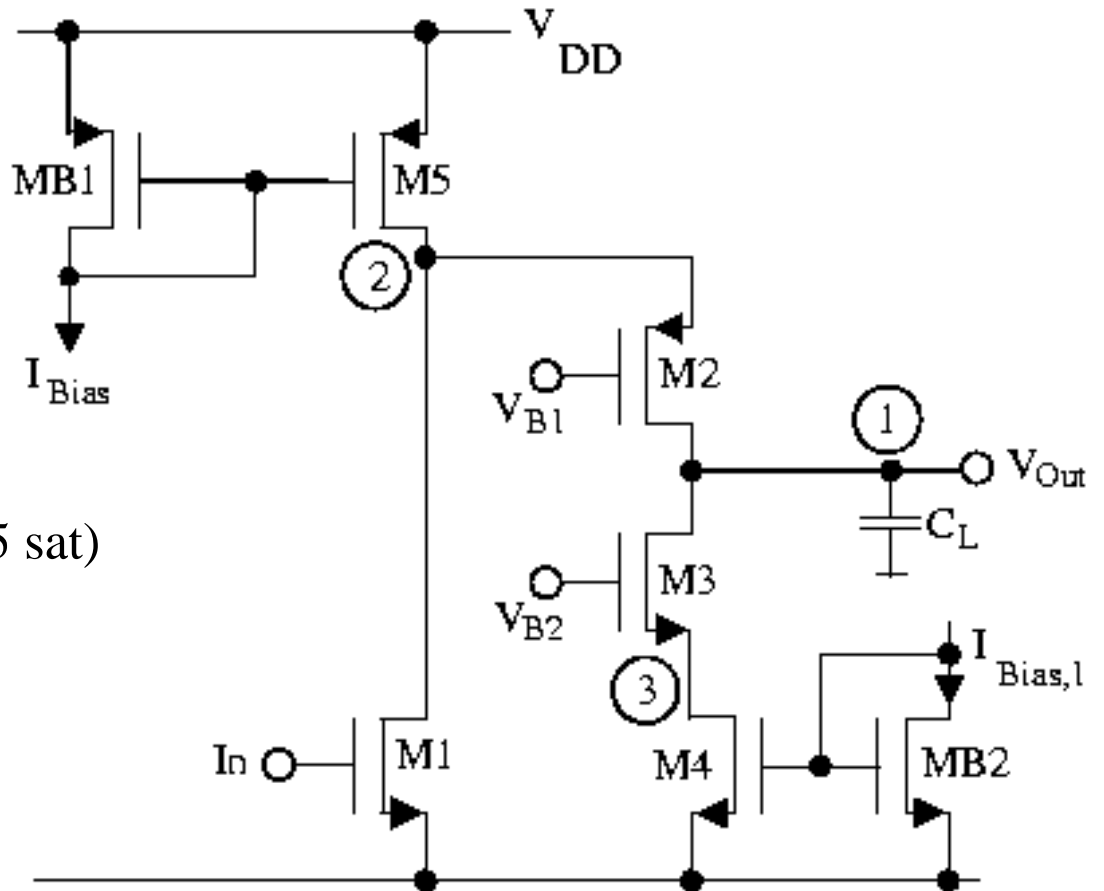
V_{B1} and V_{B2} must keep M_1

- M_5 in saturation region

$$V_{B2} > V_{sat,4} + V_{GS3} \quad (\text{for } M4 \text{ sat})$$

$$V_{B1} < V_{DD} - V_{sat,5} - V_{SG2} \quad (\text{for } M5 \text{ sat})$$

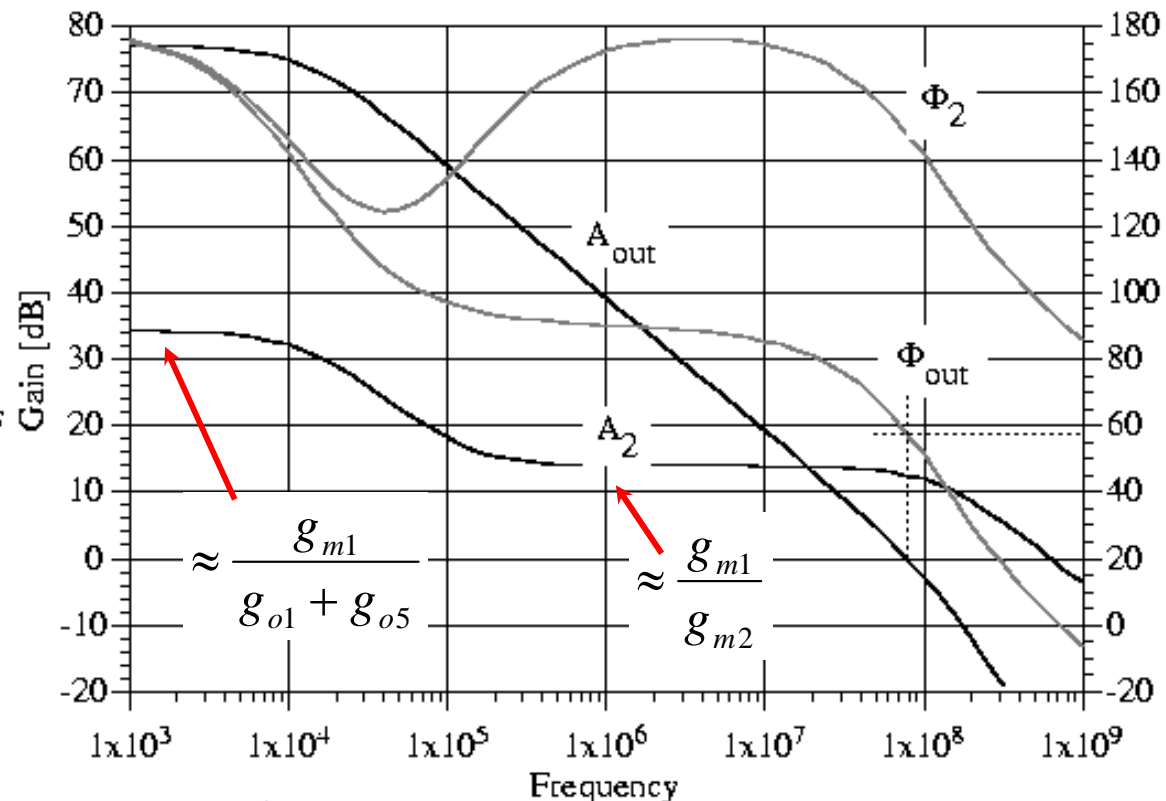
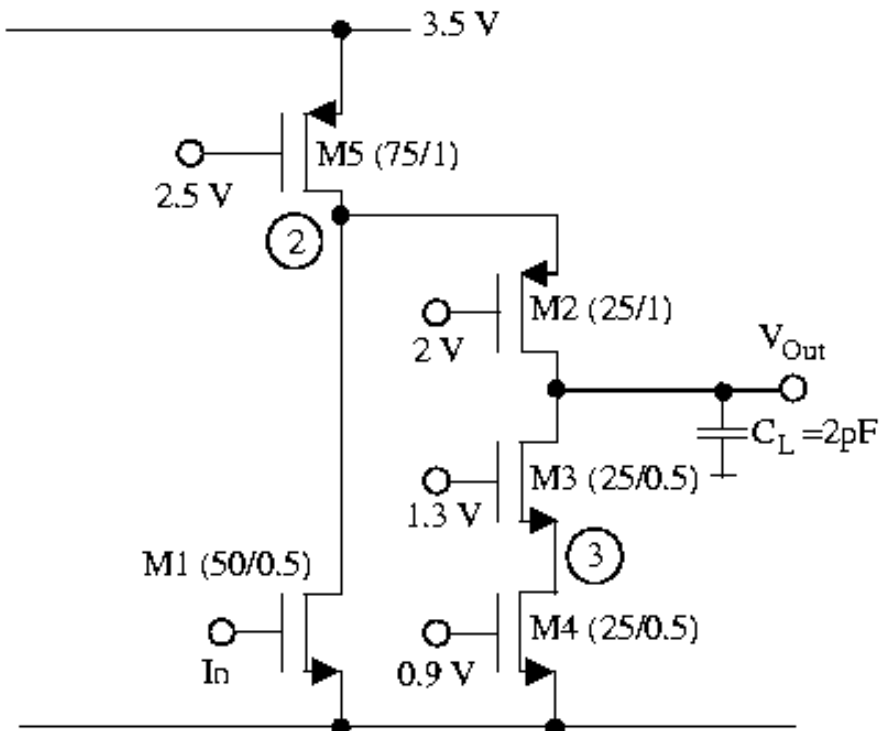
Notice that I_{D5} biases both M_2 and M_1



$$G_m = g_{m1} \quad ; \quad r_{out} \cong \left(r_{ds2} g_{m2} \left(r_{ds1} \parallel r_{ds5} \right) \right) \parallel \left(r_{ds3} g_{m3} r_{ds4} \right)$$

Example: Folded-Cascode OPAMP

Find the gain and the phase from input to output and from input to node 2.



The low frequency gain is 77 dB and the unity gain frequency is around 80 MHz.

The behavior of the gain from the input to node 2 is interesting: above the dominant pole.

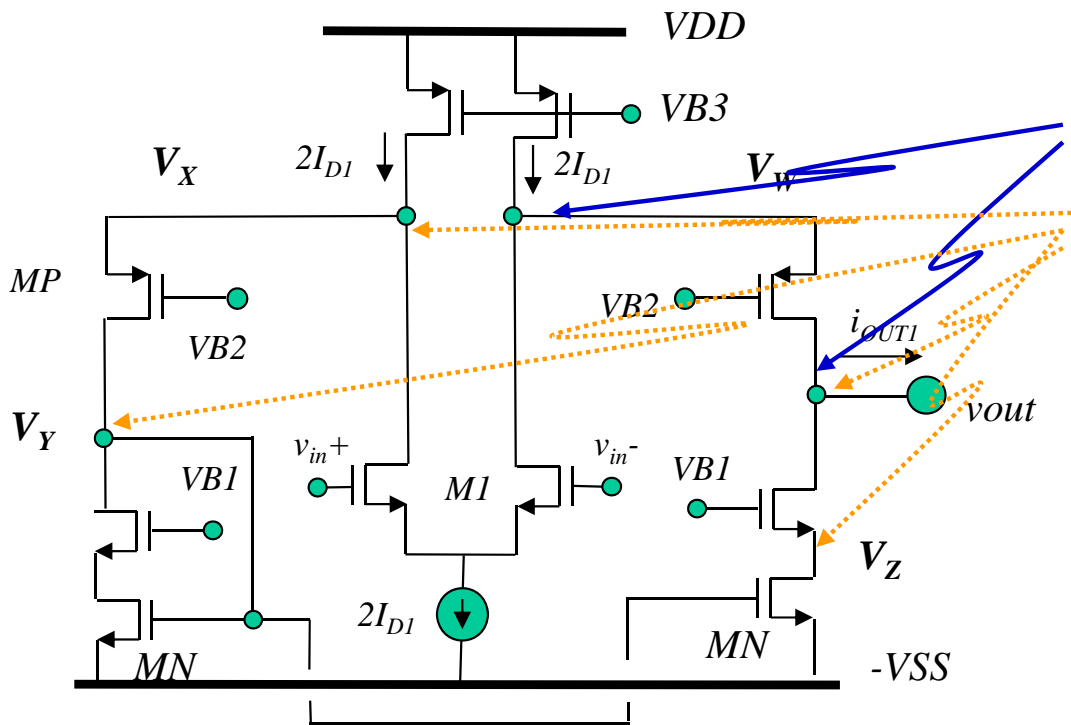
$$\omega_{z2} \approx \left(\frac{g_{m2}}{g_{o1} + g_{o5}} \right) \left(\frac{1}{r_{out} C_L} \right)$$

FOLDED-CASCODE OTA

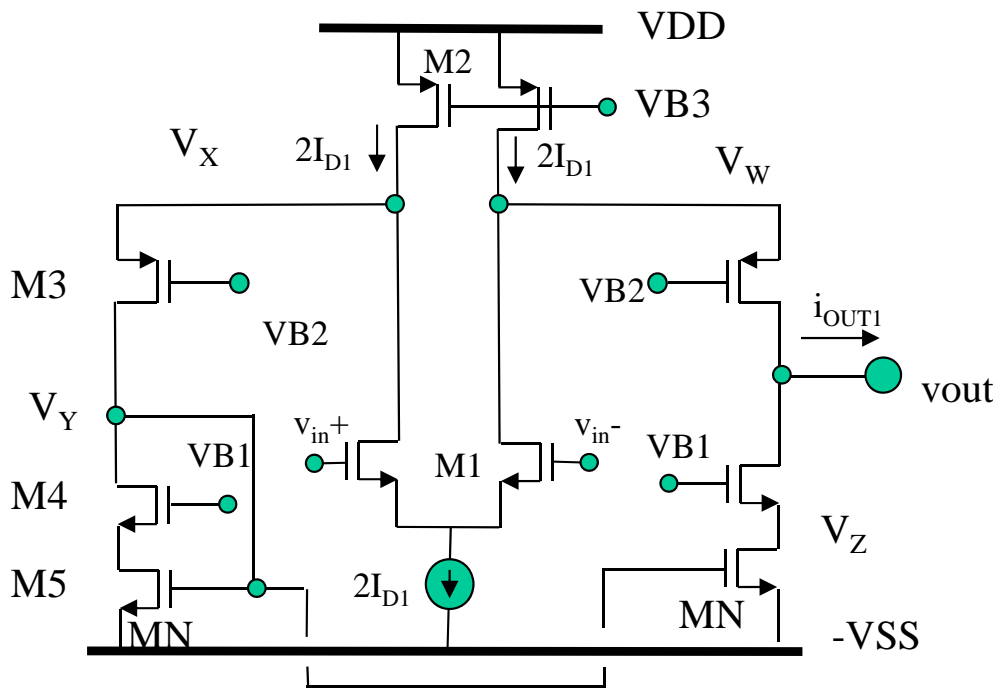
Frequency response:

Can be approximated as having 4 poles associated with nodes V_{out} , $V_{X/W}$, V_Z , and V_Y

✓ The poles at V_y and V_z are associated to N-type transistors → higher frequencies



$$A_V(s) \cong g_{m1} R_{out} * \frac{1}{1 + \frac{sC_{out}}{g_{out}}} * \frac{1}{1 + \frac{sC_{PC}}{g_{mp}}} * \frac{1}{1 + \frac{sC_Y}{g_{mn}}} * \frac{1}{1 + \frac{sC_Z}{g_{mnc}}}$$



Output referred noise

➤ M1 produces an output current given by

$$i_{01} = g_{m1} v_{n1}$$

➤ Each transistor M2 generates a differential output current

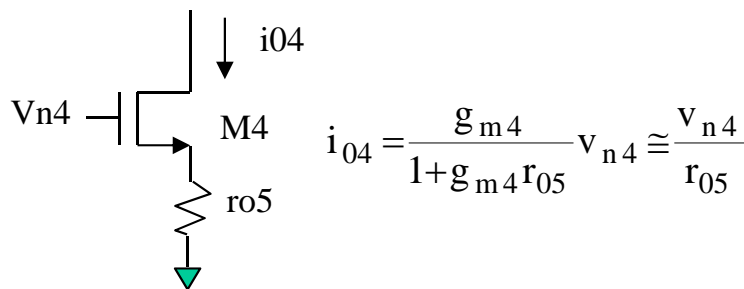
$$i_{02} = g_{m2} v_{n2}$$

➤ Similarly, for each transistor M5

$$i_{05} = g_{m5} v_{n5}$$

➤ At low and medium frequencies, noise contribution of the cascode transistors can be neglected (M3 and M4)

For cascode transistors

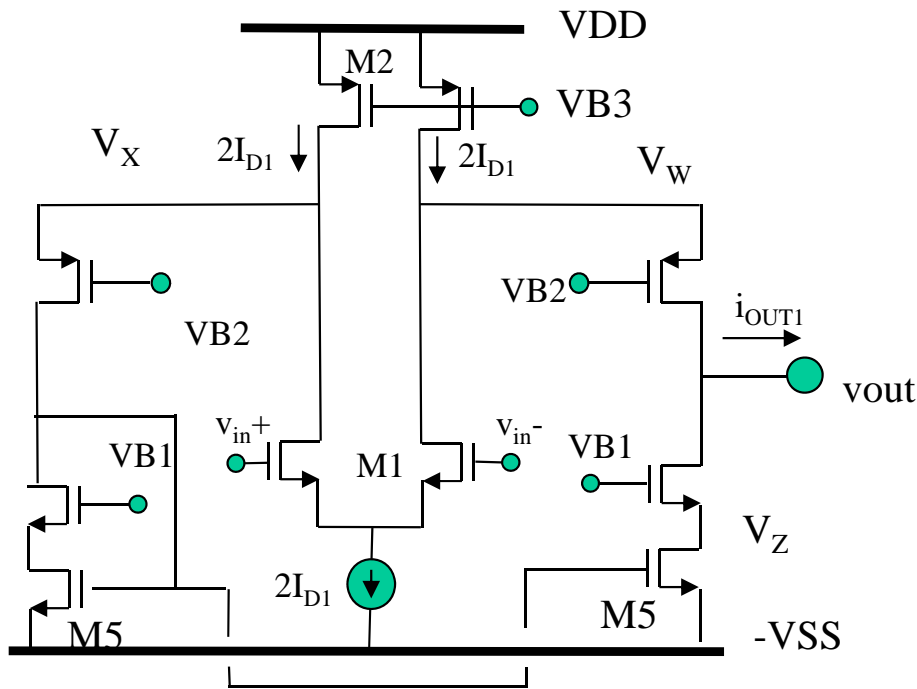


$$i_{04} = \frac{g_{m4}}{1 + g_{m4} r_{o5}} v_{n4} \approx \frac{v_{n4}}{r_{o5}}$$

Remember $i_{eq}^2 = \frac{8}{3} kT g_m$

$$i_{out}^2 = 2(i_{eq1}^2 + i_{eq2}^2 + i_{eqn}^2)$$

$$\frac{i_{out}^2}{\Delta f} = \frac{16}{3} kT (g_{m1} + g_{m2} + g_{mn})$$



Considering thermal noise only

$$\frac{v_{in}^2}{\Delta f} = \left(\frac{i_{out}^2}{\Delta f} \right) \left(\frac{1}{G_m^2} \right) = \frac{16}{3} kT (g_{m1} + g_{m2} + g_{m5}) \left(\frac{1}{g_{m1}^2} \right)$$

↓ Let's find the input rms noise

$$v_{noise} = \sqrt{\int_{BW} \frac{16}{3} kT \left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} + \frac{g_{m5}}{g_{m1}^2} \right) df}$$

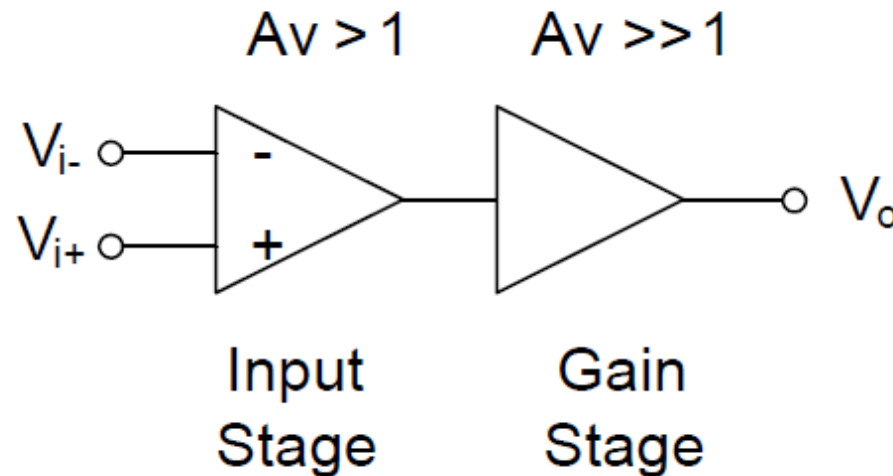
Or for a dominant (single) pole system with $NBW = (\pi/2)BW$

$$v_{noise} \approx \left(\sqrt{\frac{8kT}{g_{m1}} (BW)} \right) \left(\sqrt{1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m5}}{g_{m1}}} \right)$$

Noise of diff pair Noise Factor
(due to other transistors)

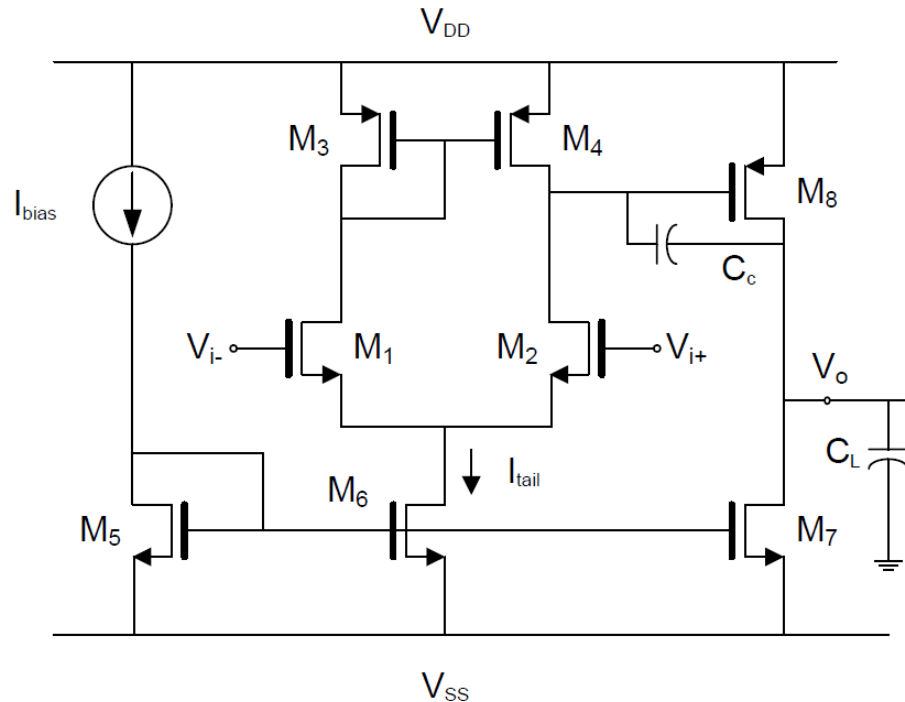
☞ **Low-noise is associated with large gm1 and relatively small gm2 and gm5**

Multi-Stage Amplifiers



- Single-stage amplifiers typically have to trade-off gain and swing range
- Multi-stage amplifiers allow for higher gain without sacrificing swing range
- The major challenge with multi-stage amplifiers is achieving adequate phase margin to insure stability in a feedback configuration

Two Stage Miller OTA



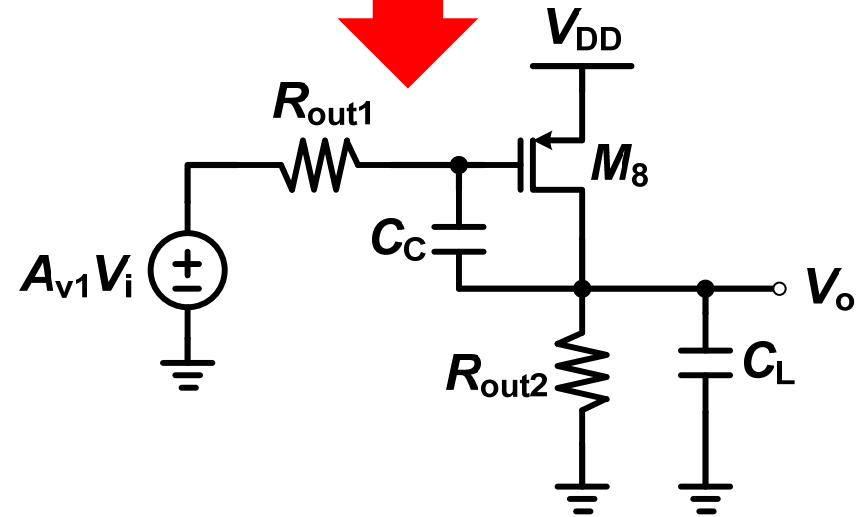
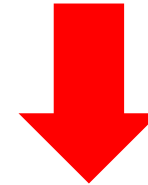
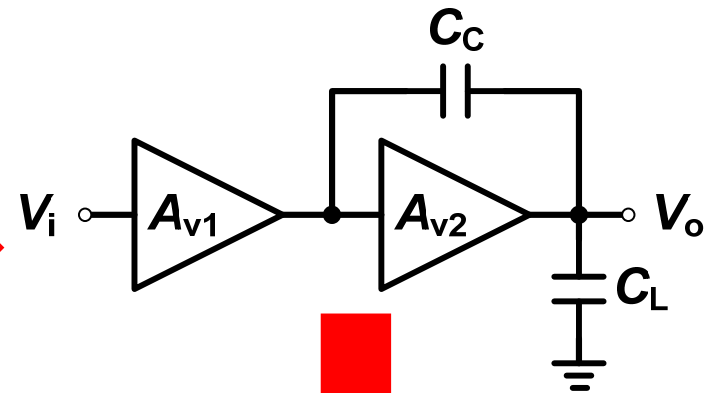
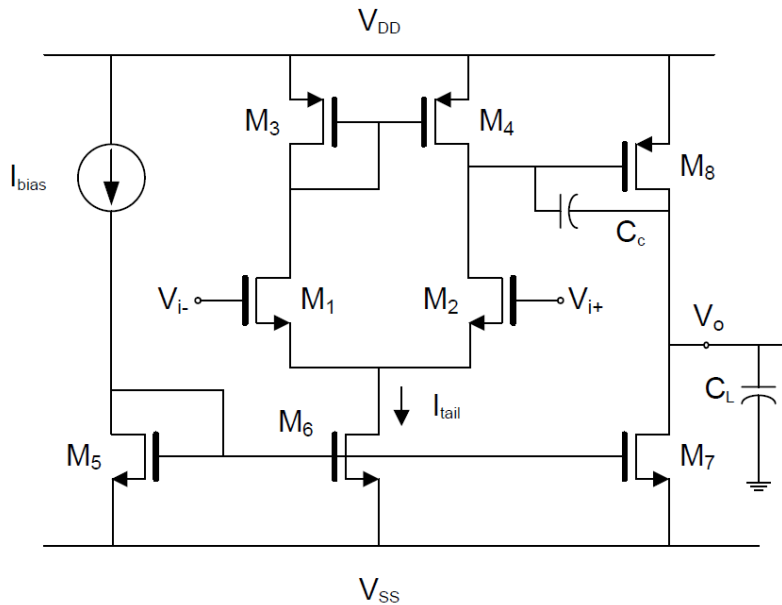
$$\text{DC Gain } A_{VDC} = A_{v1}A_{v2} = \left(-\frac{g_{m2}}{g_{o2} + g_{o4}} \right) \left(-\frac{g_{m8}}{g_{o8} + g_{o7}} \right) = \frac{g_{m2}g_{m8}}{(g_{o2} + g_{o4})(g_{o8} + g_{o7})}$$

$$A_{VDC} = G_m R_{out}$$

$$R_{out} = \frac{1}{g_{o8} + g_{o7}}$$

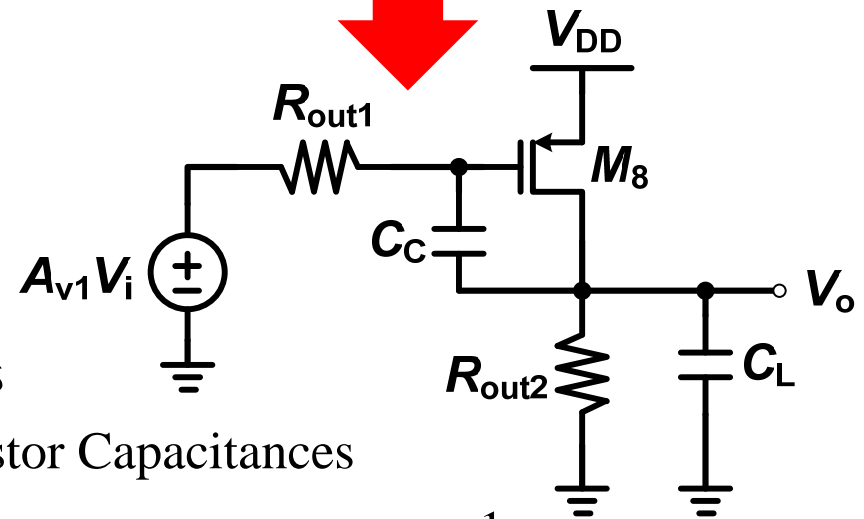
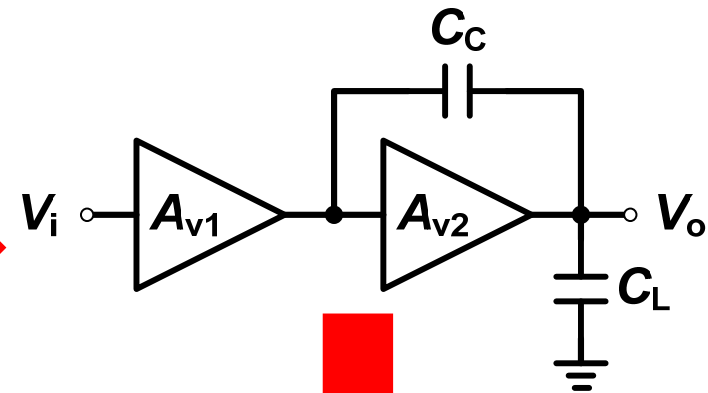
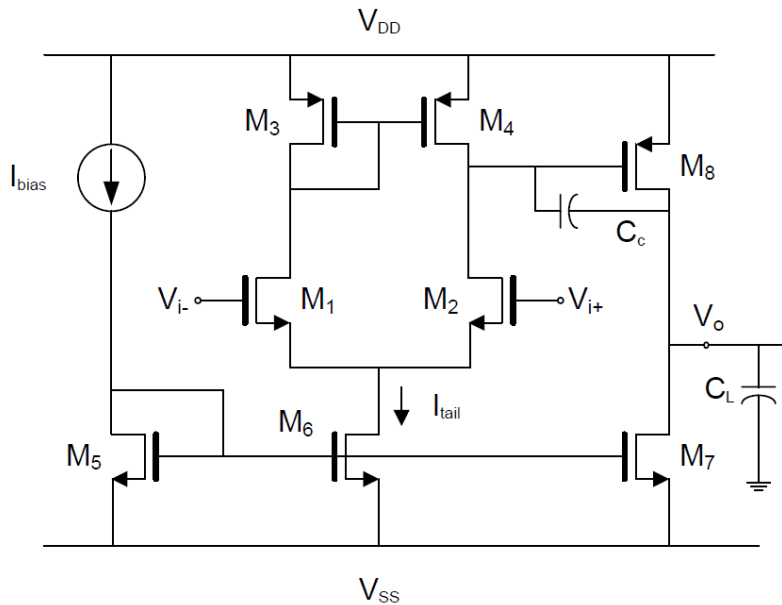
$$G_m = -g_{m8}A_{v1} = \frac{g_{m8}g_{m2}}{g_{o2} + g_{o4}}$$

Two-Stage Miller OTA – Frequency Response



- Stage 1 is a differential amplifier with an active load
- Stage 2 is a common-source amplifier with a large miller capacitor
- Using a Thevenin equivalent for Stage 1, we can use the common-source equations from Lecture 8

Two-Stage Miller OTA – Frequency Response



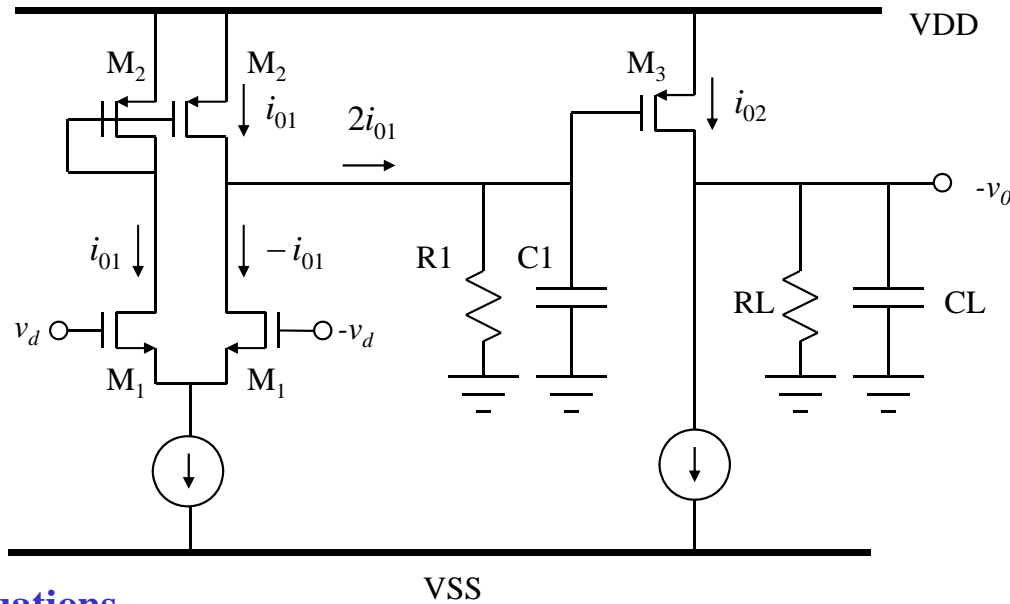
- The amplifier should be designed to yield one dominant pole, so we use the dominant pole approximation equations

Neglecting Transistor Capacitances

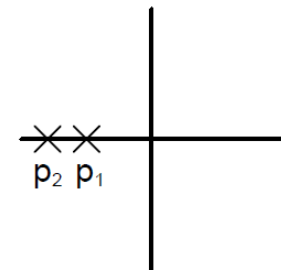
$$|\omega_{p1}| = \frac{1}{R_{out1}(1 + g_{m8}R_{out2})C_C + R_{out2}(C_C + C_L)} \approx \frac{1}{R_{out1}g_{m8}R_{out2}C_C}$$

$$|\omega_{p2}| = \frac{R_{out1}(1 + g_{m8}R_{out2})C_C + R_{out2}(C_C + C_L)}{R_{out1}R_{out2}C_C C_L} \approx \frac{g_{m8}}{C_L}$$

where $R_{out1} = r_{O2} \parallel r_{O4}$ and $R_{out2} = r_{O7} \parallel r_{O8}$



$$A(s) = \frac{A_{VDC}}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)}$$



↓ Main equations

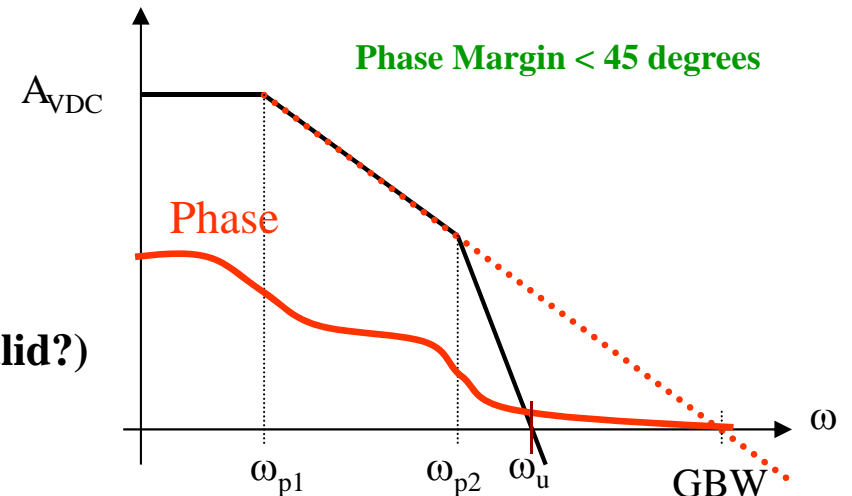
$$A_{VDC} = -\frac{g_{m1} g_{m3}}{g_1 g_L}$$

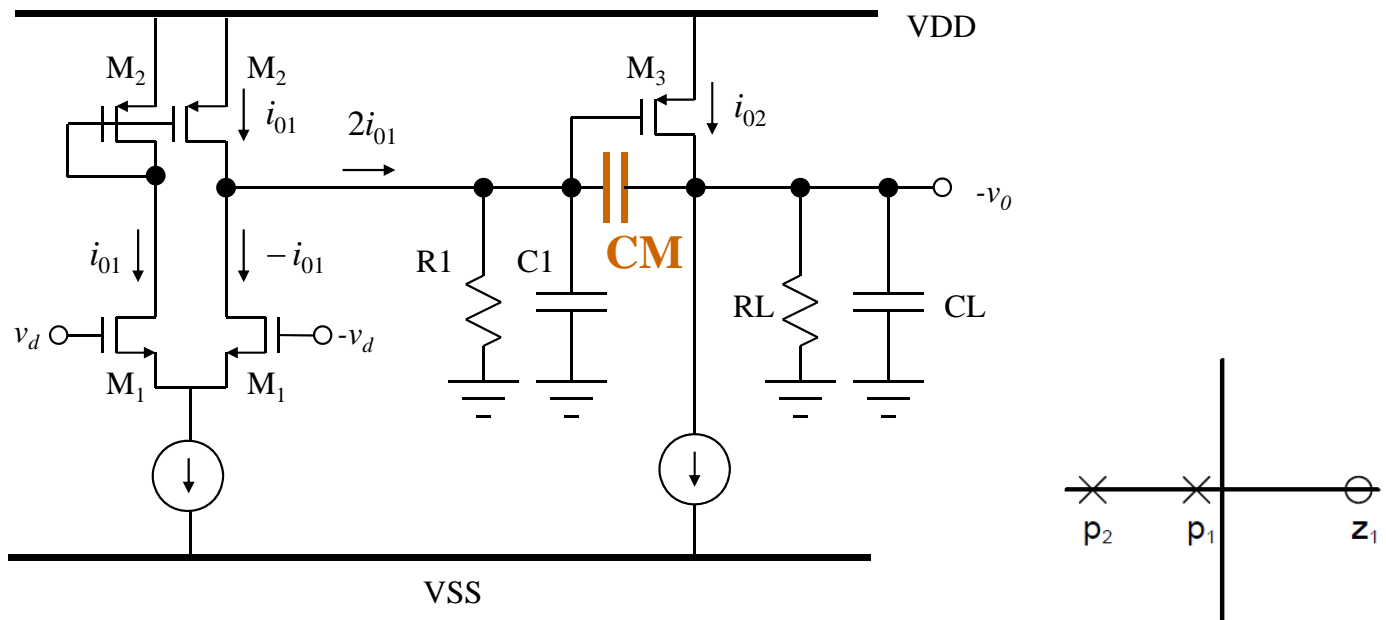
$$\omega_{p1} = -\frac{g_1}{C_1} \text{ (LHP)}$$

$$\omega_{p2} = -\frac{g_L}{C_L} \text{ (LHP)}$$

$$GBW = (A_{VDC}) * (\min(\omega_{p1}, \omega_{p2})) \text{ (if dominant pole system, valid?)}$$

$$Phase_margin = 180 - \tan^{-1}\left(\frac{\omega_u}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right)$$





$$A_{VDC} = -\frac{g_{m1}}{g_1} \frac{g_{m3}}{g_L}$$

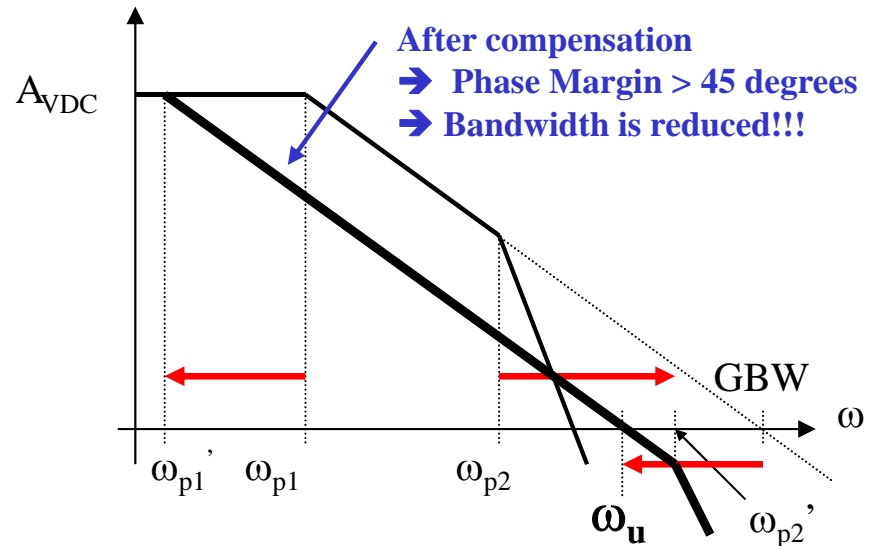
Phase compensation → Pole splitting techniques!!

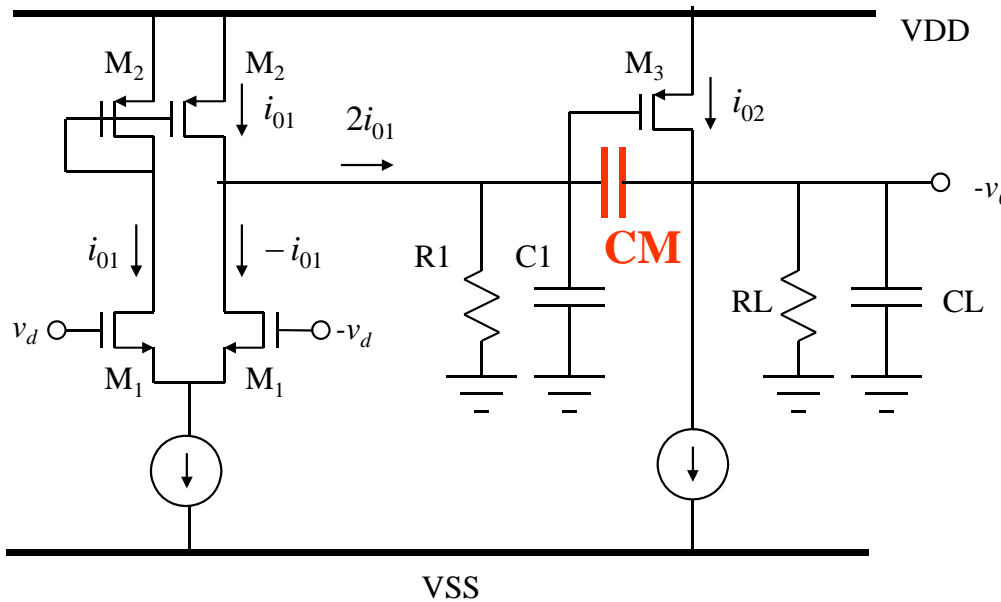
$$\omega_{p1} = -\frac{g_1}{C_1 + \frac{g_{m3}}{g_L} C_M} \quad \text{(LHP)}$$

$$\omega_{p2} = -\frac{g_{m3}}{C_1 + C_L} \quad \text{(LHP)}$$

$$GBW' = (A_{VDC}) * |\omega_{p1}| \cong \frac{g_{m1}}{C_M}$$

$$\text{Phase_margin} = 180 - \tan^{-1}\left(\frac{GBW'}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{GBW'}{\omega_{p2}}\right)$$





$$A(s) = \frac{A_{VDC} \left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)}$$

☞ **Parasitic (bad) RHP zero!!**

$$\omega_{ZERO} = + \frac{g_{m3}}{C_M} \text{ (RHP)}$$

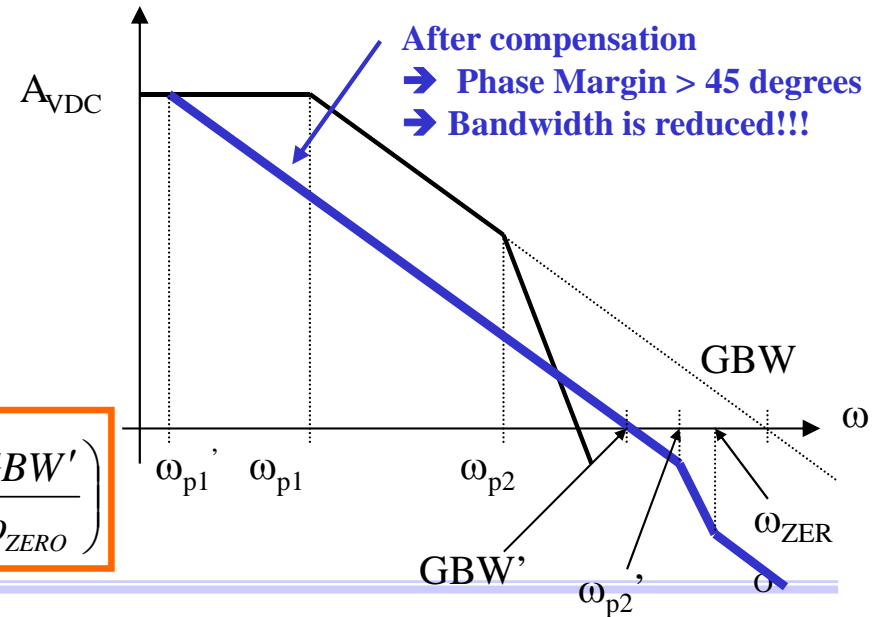
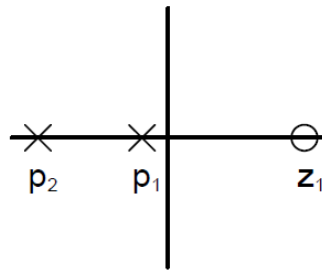
$$A_{VDC} = - \frac{g_{m1} g_{m3}}{g_1 g_L}$$

$$\omega_{p1} = - \frac{g_1}{C_1 + \frac{g_{m3}}{g_L} C_M} \text{ (LHP)}$$

$$\omega_{p2} = - \frac{g_{m3}}{C_1 + C_L} \text{ (LHP)}$$

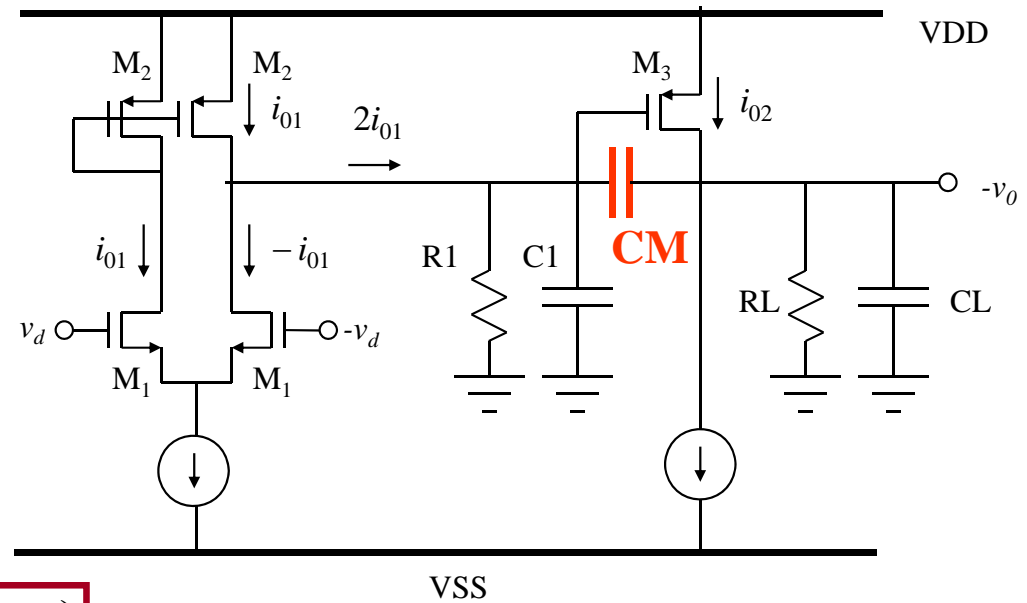
$$GBW' = (A_{VDC}) * |\omega_{p1}| \cong \frac{g_{m1}}{C_M}$$

$$Phase_margin = 180 - \tan^{-1}\left(\frac{GBW'}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{GBW'}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{GBW'}{\omega_{ZERO}}\right)$$



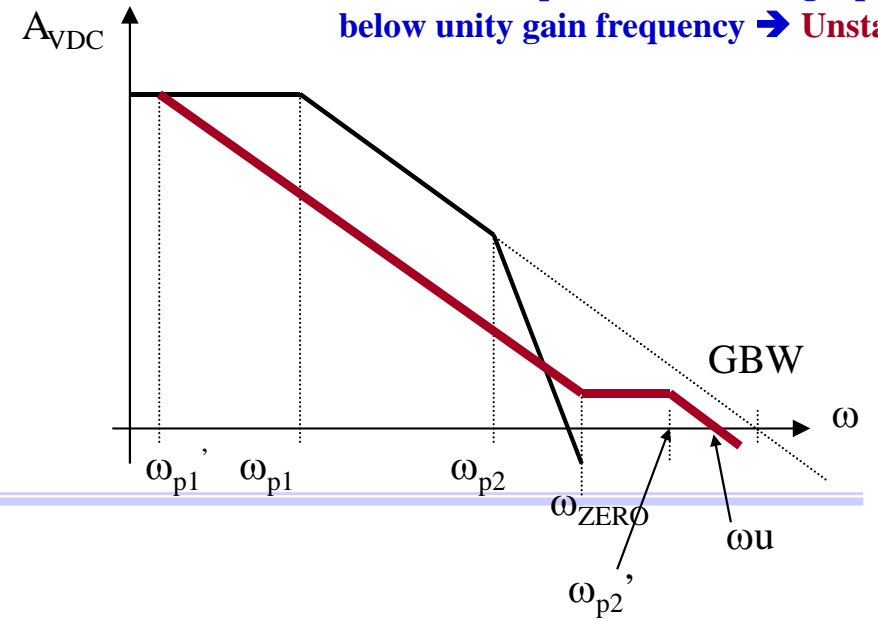
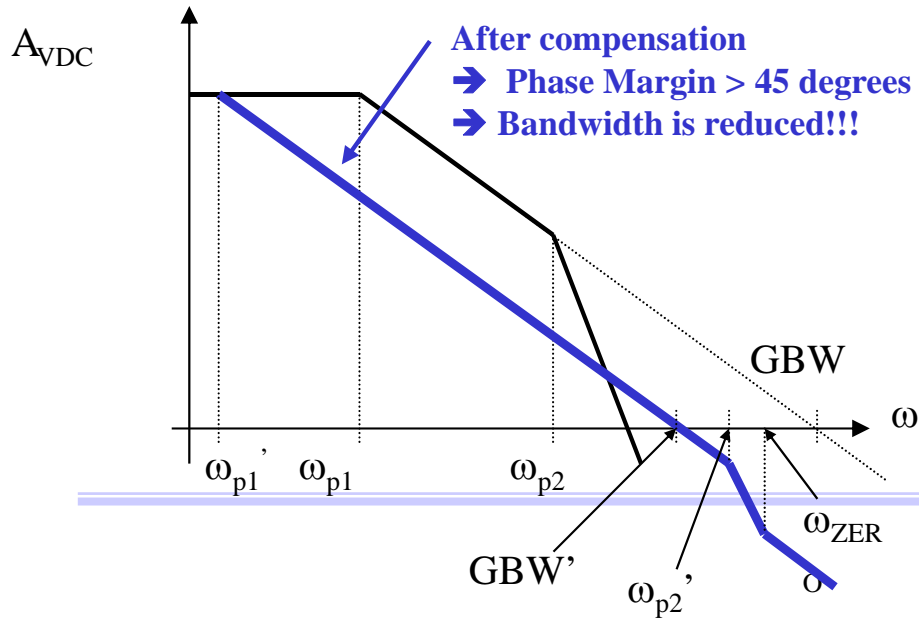
- ☞ **Parasitic (bad) RHP zero!!**
- ☞ **Can be catastrophic if close or below ω_u !**

$$\omega_{ZERO} = \frac{g_{m3}}{C_M}$$

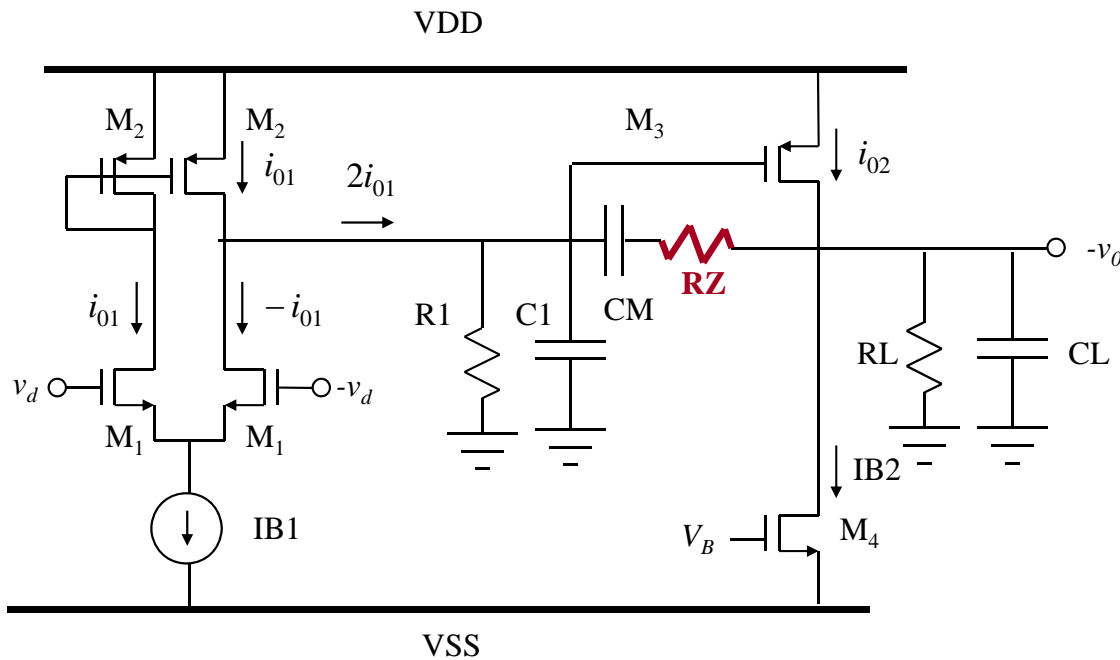


$$\text{Phase_margin} = 180 - \tan^{-1}\left(\frac{\omega_u}{\omega_{p1}'}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}'}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{ZERO}}\right)$$

After compensation
 → Phase Margin << 45 degrees
 → Phase is equivalent to having 3 poles below unity gain frequency → **Unstable!**



Adding a series resistance



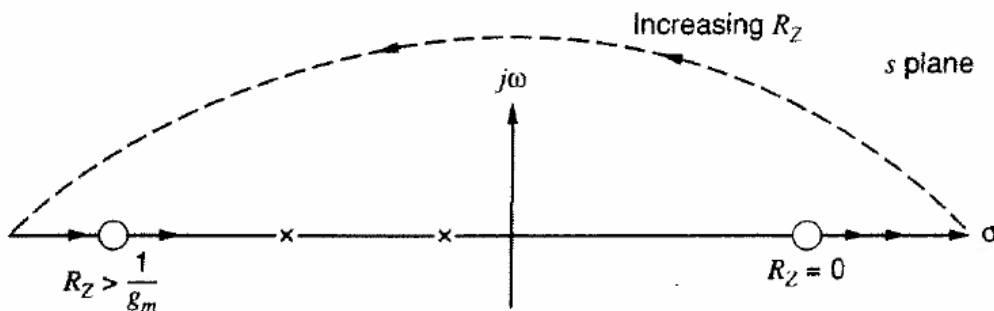
$$A(s) = \frac{A_{VDC} \left(1 - \frac{s}{\omega_z} \right)}{\left(1 + \frac{s}{\omega_{p1}} \right) \left(1 + \frac{s}{\omega_{p2}} \right) \left(1 + \frac{s}{\omega_{p3}} \right)}$$

$$\omega_{p3} \approx -\frac{1}{R_Z C_1} \quad (\text{Generally high frequency \& can be ignored})$$

$$\omega_z = \frac{1}{\left(\frac{1}{g_{m3}} - R_Z \right) C_M}$$

Can design R_Z to improve phase margin

Non - zero R_Z will push RHP to a higher frequency (initially)

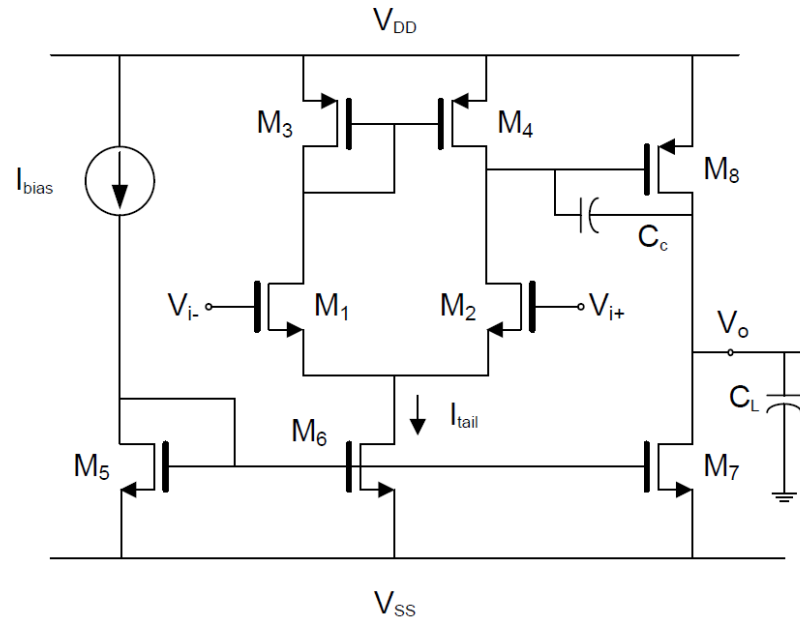


$$R_Z = \frac{1}{g_{m3}} \quad \text{pushes the RHP zero to infinity}$$

$$R_Z > \frac{1}{g_{m3}} \quad \text{pushes zero from RHP to LFP}$$

$$R_Z = \frac{C_L + C_M + C_1}{g_{m3} C_M} \quad \text{can cancel } \omega_{p2}$$

Two Stage Miller OTA Noise



Output - Referred Noise Current PSD

$$\frac{i_o^2}{\Delta f} = \frac{8kT}{3} \left[g_{m8} + g_{m7} + 2g_{m2} \left(\frac{g_{m8}}{g_{o2} + g_{o4}} \right)^2 + 2g_{m4} \left(\frac{g_{m8}}{g_{o2} + g_{o4}} \right)^2 \right]$$

Input - Referred Noise Voltage PSD

$$\frac{v_i^2}{\Delta f} = \frac{i_o^2}{\Delta f} \left(\frac{1}{G_m^2} \right) = \frac{8kT}{3g_{m2}} \left[2 + 2g_{m4} + \frac{g_{m8} + g_{m7}}{g_{m2} \left(\frac{g_{m8}}{g_{o2} + g_{o4}} \right)^2} \right]$$

Next Time

- OpAmp Feedback & Stability
- Common-Mode Feedback Techniques