ECEN474/704: (Analog) VLSI Circuit Design Spring 2018

Lecture 16: Output Stages

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Announcements

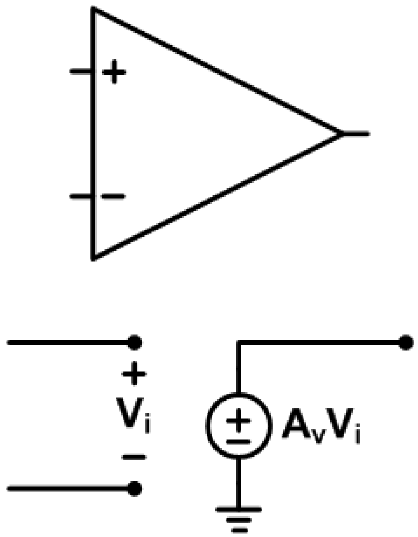
- Project Report Due May 1
  - Email it to me by 5PM
- Exam 3 is on May 3
  - 3PM-5PM
  - Closed book w/ one standard note sheet
  - 8.5″x11″ front & back
  - Bring your calculator
  - Covers material through Output Stages Lecture
  - Previous years' exam 3s are posted on the website for reference

Agenda

- Output Stages
  - Source Follower (Class A)
  - Push-Pull (Class B)
  - Push-Pull w/ Small Quiescent Current (Class AB)

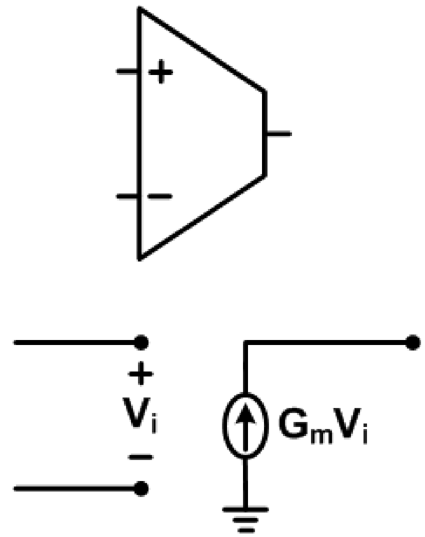
OpAmps and OTAs

OpAmp



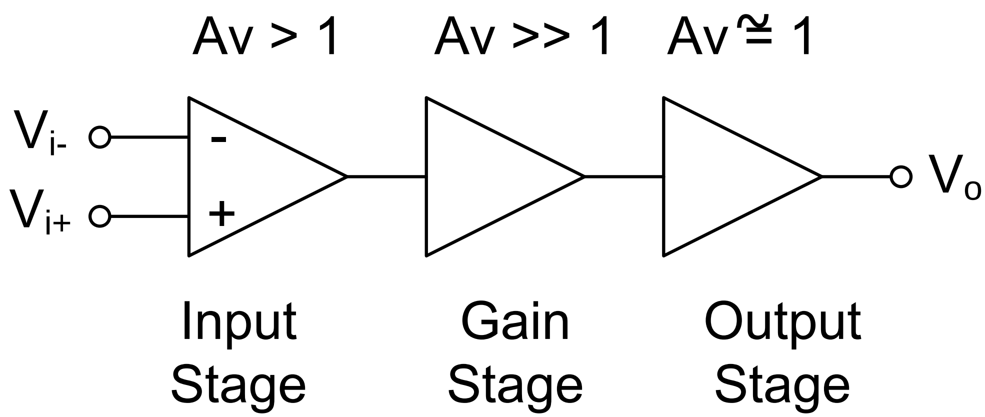
- High voltage gain
- High input impedance
- Voltage source output (low impedance)

OTA



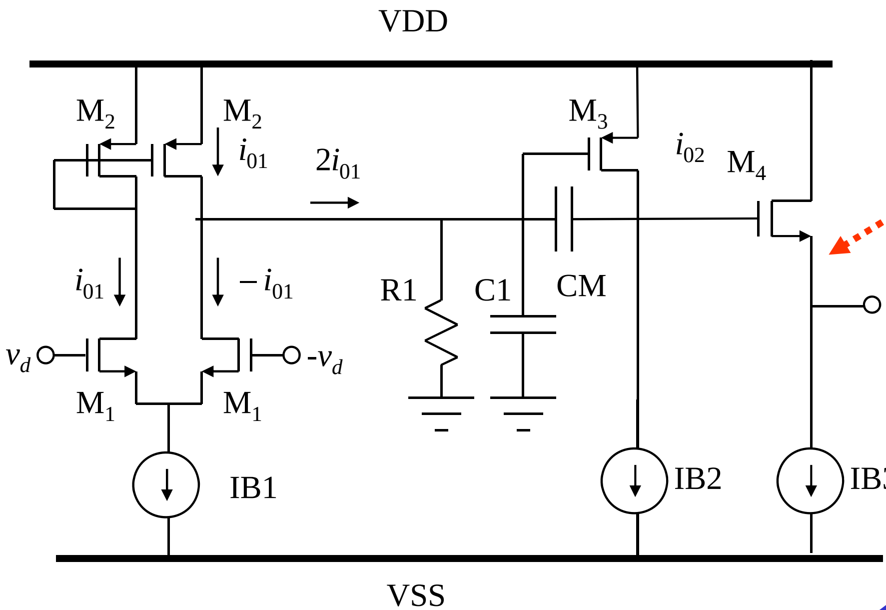
- High “voltage” gain
  - As long as it’s driving a high impedance load (capacitor)
- High input impedance
- Current source output (high impedance)

Three-Stage OpAmp

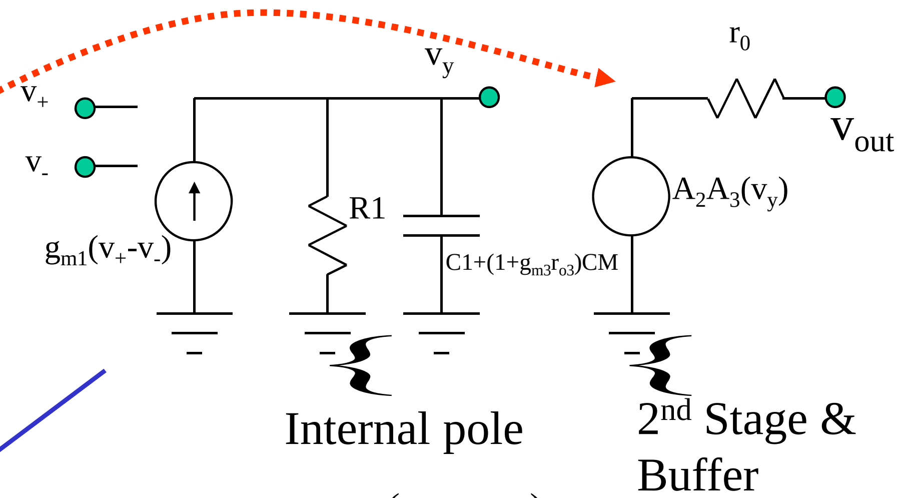


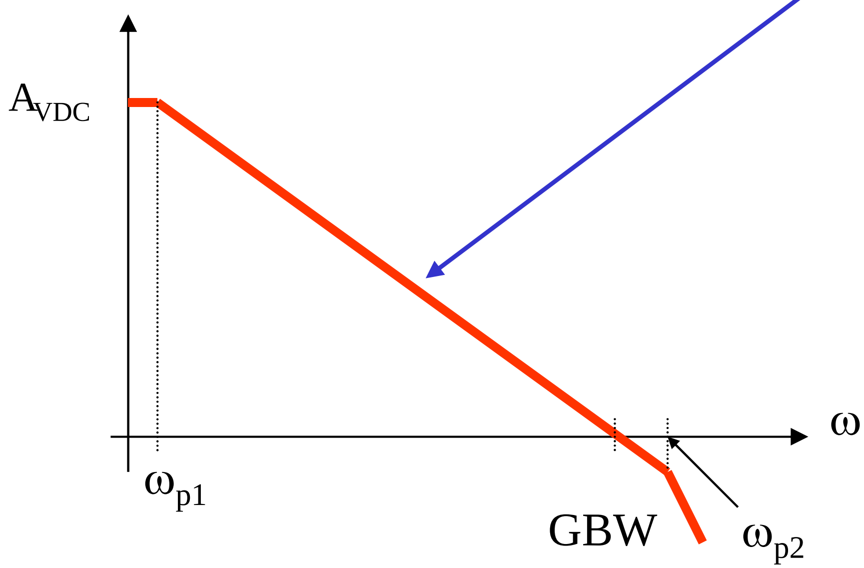
- Differential input stage
  - Amplifies differential input
  - Sets specs such as G_m, CMRR, and slew rate
- Second gain stage
  - Provides additional gain
  - Often used to provide Miller compensation
- Output stage
  - "Power Amplifier"
  - Large current gain and near unity voltage gain
  - Small output impedance

Buffered OTA = Operational Voltage Amplifier (OPAMP)



SIMPLE MACROMODEL:





$$A_{VDC} = (g_{m1}R_1)A_2A_3$$

$$A_2 \approx g_{m3}r_{o3}$$

$$A_3 \approx 1 - 0.5$$

$$GBW \cong \frac{g_{m1}}{C_M}$$

$$R_{out} = r_0 \cong 1/g_{m4}$$

➔Notice that load capacitors must satisfy the following condition, otherwise phase margin is not good enough

$$GBW < \frac{1}{r_0C_L}$$

Source Follower (Class A) Output Stage

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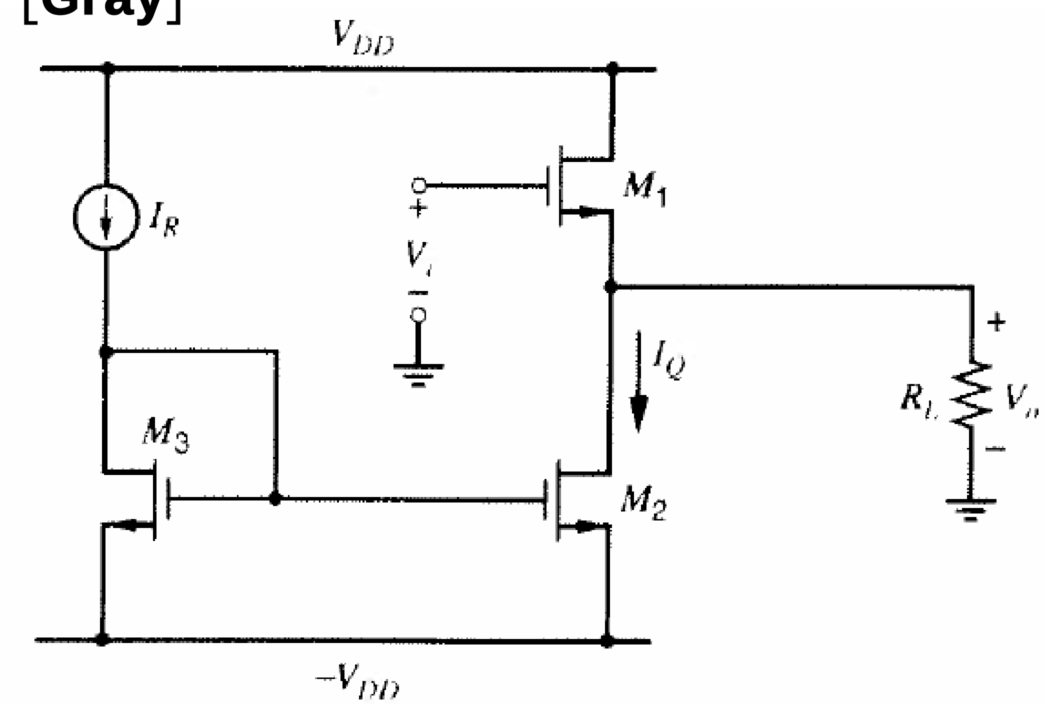
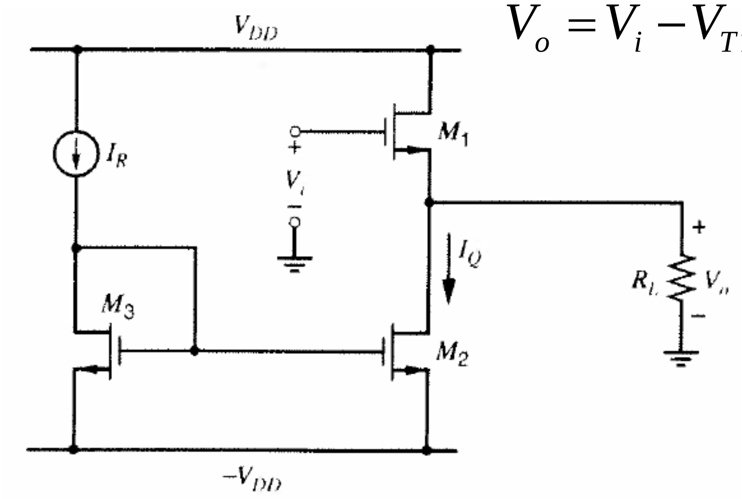


- Voltage gain close to 1
- Low output resistance
- DC level shift of V_{GS1}
- Class A output stage transistors conduct current over an entire input cycle

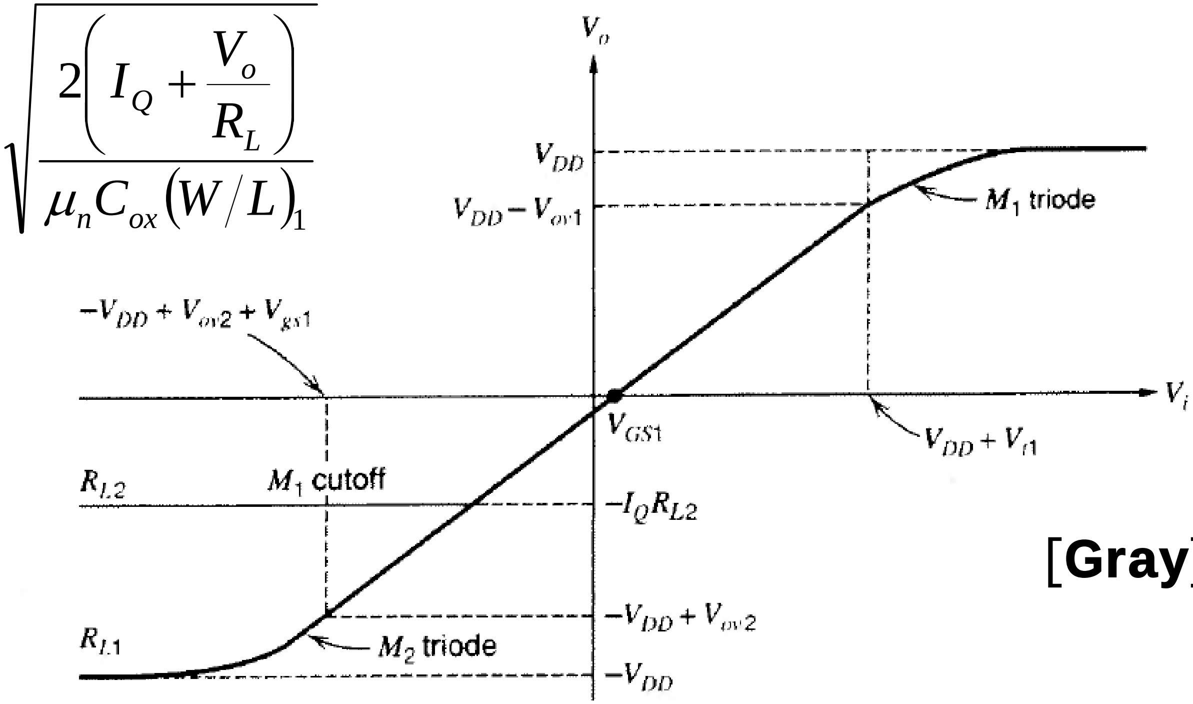
$$A_{dc} = \frac{g_{m1}}{g_{m1} + g_{o1} + g_{mb1} + g_{o2} + g_L} \approx \frac{g_{m1}R_L}{1 + g_{m1}R_L} \approx \mathbf{1} \quad \textbf{(Optimistic)}$$

$$R_{out} = \frac{1}{g_{m1} + g_{o1} + g_{mb1} + g_{o2}} \approx \frac{1}{g_{m1}}$$

Source Follower (Class A) Transfer Characteristic



$$V_o = V_i - V_{T1} - \sqrt{\frac{2\left(I_Q + \frac{V_o}{R_L}\right)}{\mu_n C_{ox}(W/L)_1}}$$



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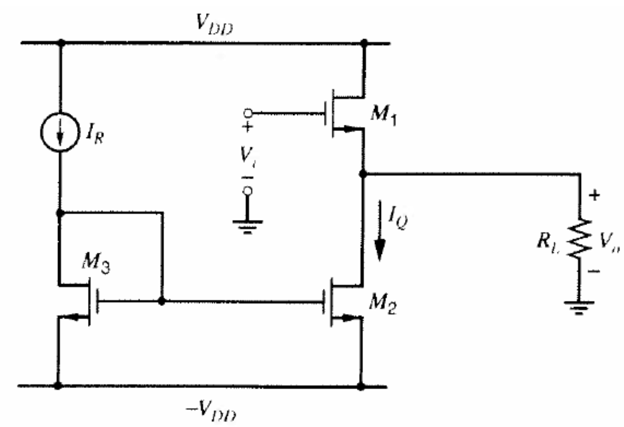
- Maximum V_o is set by M1 saturation condition
  - If $V_{in} \leq V_{DD}$, then Maximum $V_o = V_{DD}\text{-}V_{GS1}$
  - Output transistors remain in saturation up to $V_o = V_{DD}\text{-}V_{DSAT1}$ if V_{in} swings up to $V_{DD}+V_{T1}$
- Minimum V_o depends on R_L
  - For small R_L (heavy load), M1 gets cutoff and $V_o \geq -I_Q R_L$
  - For large R_L (light load), M2 will go into triode region at $-V_{DD}+V_{DSAT2}$

Source Follower (Class A) Power Efficiency



Assuming a sinusoidal output voltage

$$V_o = V_m \sin(\omega t)$$

The power delivered to the load at the signal frequency ω is

$$P_{ac} = \frac{\left(\frac{V_m}{\sqrt{2}}\right)^2}{R_L} = \frac{V_m^2}{2R_L}$$

The average power consumed by the source follower is

$$P_{av} = (-I_Q)(-V_{DD}) + (I_Q)(V_{DD}) = 2I_Q V_{DD}$$

The output stage power efficiency is

$$P_{eff} \equiv \frac{P_{ac}}{P_{av}} = \frac{V_m^2}{4R_L I_Q V_{DD}}$$

Maximum power efficiency is achieved when the output amplitude approaches V_{DD} and I_Q is designed to be $\frac{V_{DD}}{R_L}$

$$\text{Max } P_{eff} = \frac{1}{4} \text{ or } 25\% \text{ (not that good!)}$$

Super Buffer Output Stage

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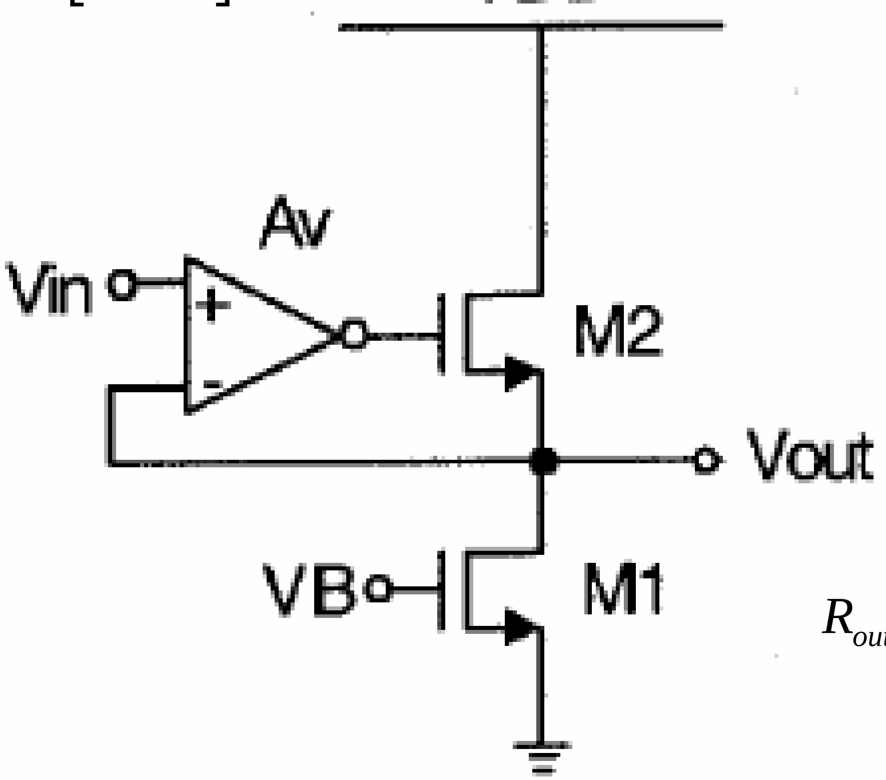
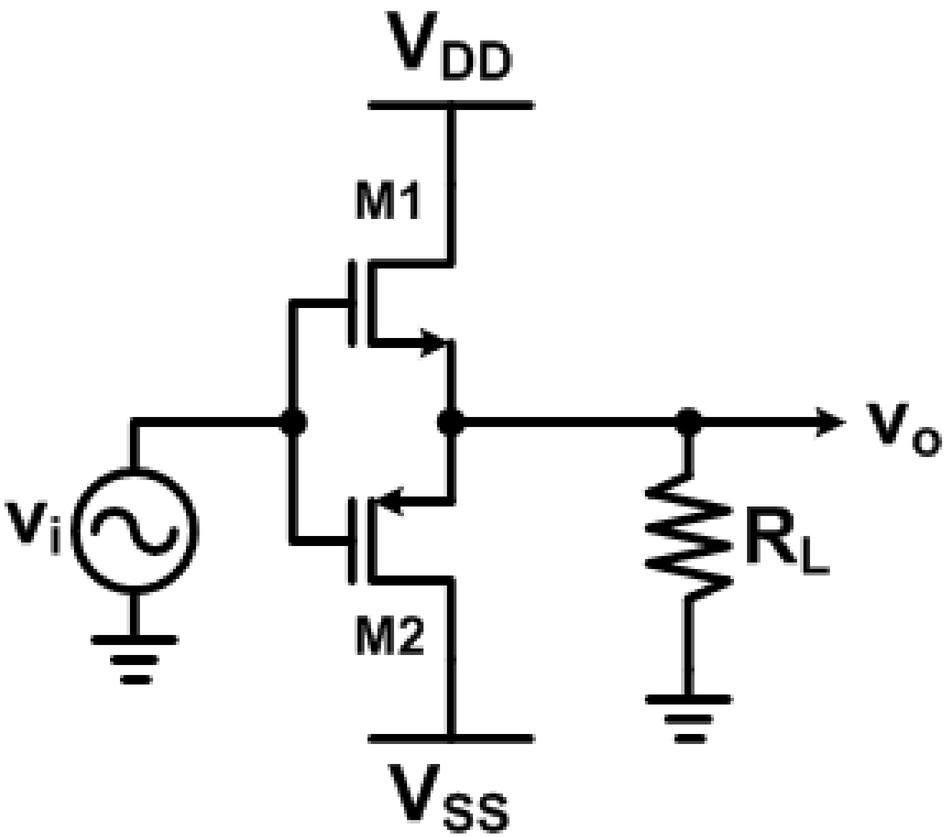


$$R_{out} \approx \frac{1}{g_{m2}\left(1 + A_v\right)}$$

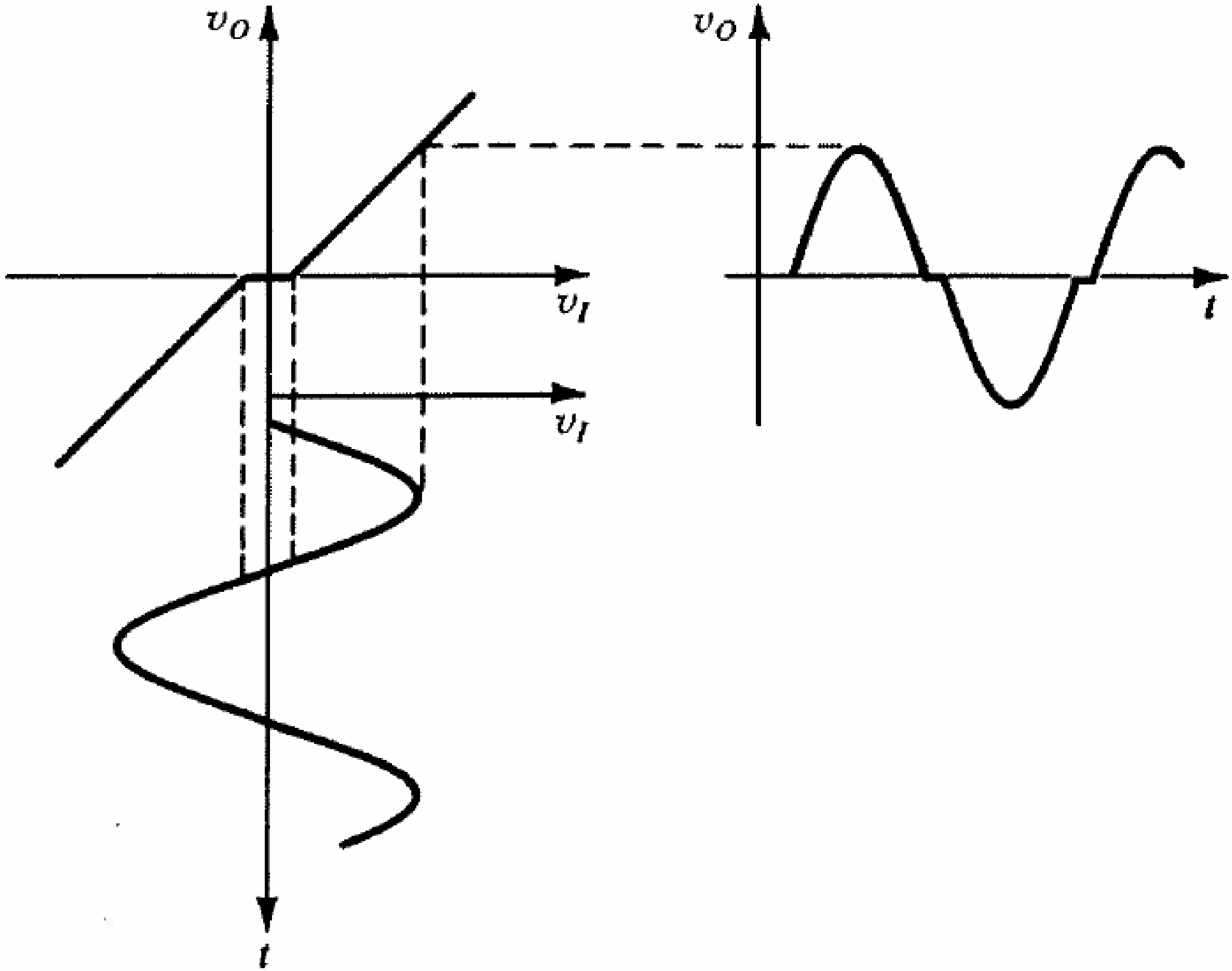
- Employs a “gain-boosting” technique where the effective transcoductance of M2 is boosted by 1-A_v, where A_v is the gain from the source-to-gate, which should be negative for stability
- Results in an output resistance reduction by a 1/(1+A_v) factor

Push-Pull Source Follower (Class B) Output Stage



- Class B output stages have only one transistor conducting current for each half cycle
  - M1 during positive half
  - M2 during negative half
- Results in improved power efficiency by operating at zero quiescent current
- However, if
  $-|V_{TP}| \leq V_{in} \leq V_{TN}$,
  then no output signal

Push-Pull Source Follower (Class B) Crossover Distortion



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Push-Pull Source Follower (Class B) Power Efficiency

Assuming a sinusoidal output voltage

$$V_o = V_m \sin(\omega t)$$

The power delivered to the load at the signal frequency ω is

$$P_{ac} = \frac{\left(\frac{V_m}{\sqrt{2}}\right)^2}{R_L} = \frac{V_m^2}{2R_L}$$

The current consumed by the push - pull stage from the two supplies

consists of half - sine wave of peak amplitude $\frac{\mathbf{V_m}}{\mathbf{R_L}}$

The average current will be $\frac{V_m}{\pi R_L}$

$$P_{av} = \left(-\frac{V_m}{\pi R_L}\right)(-V_{DD}) + \left(\frac{V_m}{\pi R_L}\right)(V_{DD}) = \frac{2V_m V_{DD}}{\pi R_L}$$

The output stage power efficiency is

$$P_{eff} \equiv \frac{P_{ac}}{P_{av}} = \frac{\pi V_m}{4V_{DD}}$$

Maximum power efficiency is achieved when the output amplitude approaches $\mathbf{V_{DD}}$

Max $\mathbf{P_{eff}} = \frac{\pi}{4}$ or 78.5% (much better!)

Push-Pull w/ Small Quiescent Current (Class AB) Output Stage

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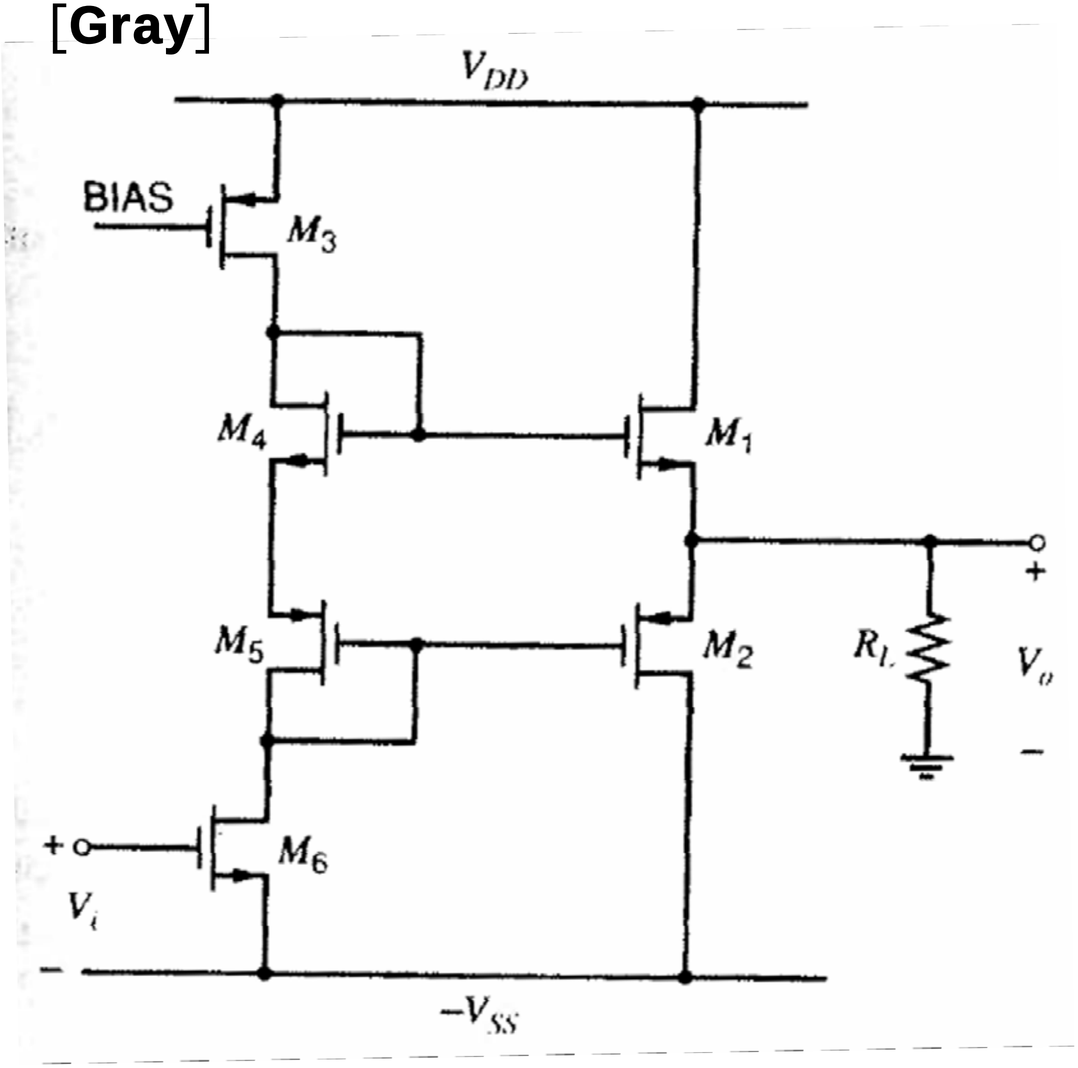

- Power efficiency of the Class-B output stage is great, but the crossover distortion is a major issue
- Solution to the crossover distortion is to bias the transistors into conduction at a low quiescent current
- Level-shift transistors M4 and M5 are sized such that V_{GS1} and V_{SG2} are slightly larger than their threshold voltages

Push-Pull w/ Small Quiescent Current (Class AB) Output Swing Range

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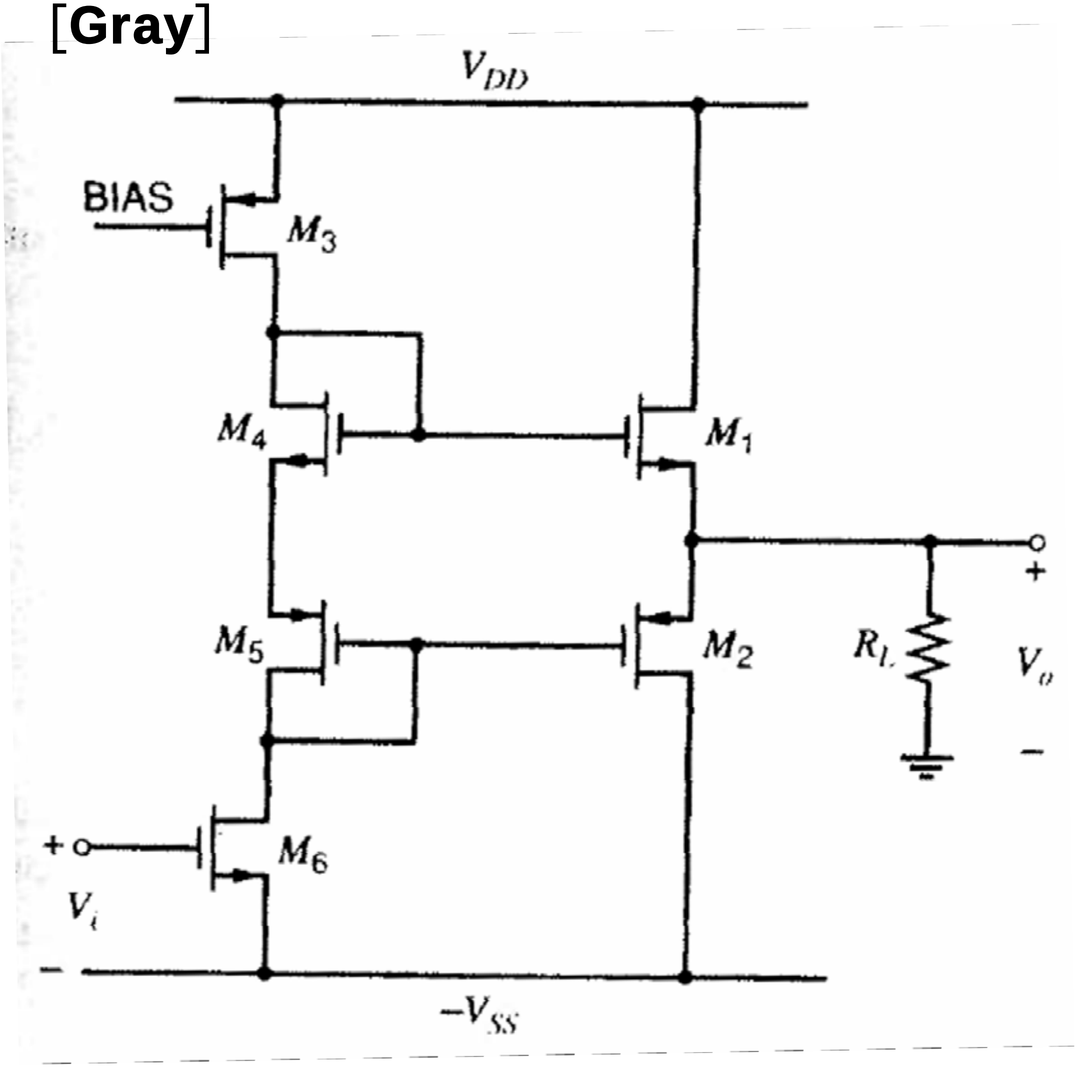

- A drawback of the CMOS Class AB output stage is the limited output swing range
- Maximum V_o set by M1 source follower
  - $V_o \le V_{DD} - |V_{DSAT3}| - V_{GS1}$
- Minimum Vo set by M2 source follower
  - $V_o \ge -V_{SS} + V_{DSAT6} + V_{SG2}$

Next Time

- Bandgap Reference Circuits