ECEN620: Network Theory
Broadband Circuit Design
Fall 2014

Lecture 14: Fractional-N Frequency Synthesizers

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Announcements

• HW4 Due Wednesday Nov 5
• Exam 2 Friday Nov 7
  • One double-sided 8.5x11 notes page allowed
  • Bring your calculator
  • Covers through Lecture 14
Agenda

• PLL Bandwidth and Frequency Resolution Trade-Offs
• Fractional-N Frequency Synthesizers
• Modulus Randomization and Noise Shaping
PLL Bandwidth Constraints

- PLL loop bandwidth should be \(<0.1*f_{\text{ref}}\) in order to maintain loop stability
  - Continuous-time model breaks down if loop bandwidth is too high
Issues with Synthesizing Frequencies at a Tight Channel Spacing

• In a simple integer-N PLL, the output frequency resolution is equal to the input reference frequency.
Issues with Synthesizing Frequencies at a Tight Channel Spacing

- In integer-N PLLs, synthesizing tight channel spacings requires extremely low effective reference frequencies
- This results in very low loop bandwidths and high divide ratios
  - Slow PLL frequency switching time
  - Large area passives
  - High phase noise at low frequencies
Fractional-N Frequency Synthesizers

- A fractional-N frequency synthesizer allows the effective division ratio to take on a fractional value.
- The output frequency can then be at a much higher resolution than the reference frequency.
- Allows a higher loop bandwidth.

\[ \frac{\theta}{\theta} \frac{(N+1)}{N} \]
Effective Divide Ratio

\[ N_{\text{eff}} = \frac{A + B}{\frac{A}{N} + \frac{B}{N + 1}} \]

where \( A \) is the number of VCO cycles divided by \( N \) and

\( B \) is the number of VCO cycles divided by \( N + 1 \)

Example: To realize an effective divide ratio of 4.25,

divide by 4 three times (12 VCO cycles) and 5 once (5 VCO cycles)

\[ N_{\text{eff}} = \frac{A + B}{\frac{A}{N} + \frac{B}{N + 1}} = \frac{12 + 5}{\frac{12}{4} + \frac{5}{5}} = \frac{17}{4} = 4.25 \]
Dual Modulus Prescalers

\[ \frac{\text{MC}=0}{2/3} \quad \frac{\text{MC}=1}{2} \]

Synchronous \( \div 3/4 \)
- For \( /15 \), first prescaler circuit divides by 3 once and 4 three times during the 15 cycles

Asynchronous \( \div 4 \)

[Razavi]
Phase Error with Simple Periodic Modulus Control

- As only the average of the feedback frequency is equal to the reference frequency, the phase error will accumulate over N reference cycles before being reset.

[Perrott]
Fractional-N Frequency Synthesizer Spurs

- Simple periodic modulus control causes a ramp-type phase error accumulation over N reference cycles
- This is translated into periodic disturbances in the VCO control voltage, which causes relatively close-in spurs in the frequency domain
• Instead of periodically changing the divider modulus, randomly switch it such that the average division factor still yields the desired fractional value.

• This converts the systematic fractional spurs into random noise.
Including Noise Shaping in Modulus Control

- This technique can be extended by in addition to randomization, shaping the noise in such a way that it can be filtered by the PLL.
Sigma-Delta Modulation Noise Shaping

- High-pass noise shaping can be realized by using a sigma-delta modulator for modulus control.
- The divider quantization noise can then be filtered by the PLL more efficiently.

Delta–Sigma Modulation in Fractional-$N$ Frequency Synthesis

Tom A. D. Riley, Member, IEEE, Miles A. Copeland, Fellow, IEEE, and Tad A. Kwasniewski, Member, IEEE
Next Time

• Delay-Locked Loops (DLLs)

• Clock-and-Data Recovery Systems