Lecture 16: CDRs
Announcements

• Project descriptions are posted on the website
  • Preliminary report due 11/21 and will count as the final homework
Agenda

• CDR overview
• CDR phase detectors
• Analog & digital CDRs
• Dual-loop CDRs
• CDR jitter properties
Embedded Clock I/O Circuits

- TX PLL
- TX Clock Distribution
- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
  - Global PLL requires RX clock distribution to individual channels
Clock and Data Recovery

- A clock and data recovery system (CDR) produces the clocks to sample incoming data.
- The clock(s) must have an effective frequency equal to the incoming data rate:
  - 10GHz for 10Gb/s data rate
  - OR, multiple clocks spaced at 100ps
  - Additional clocks may be used for phase detection
- Sampling clocks should have the proper phase relationship with the incoming data for sufficient timing margin to achieve the desired bit-error-rate (BER).
- CDR should exhibit small effective jitter.
Embedded Clocking (CDR)

- Clock frequency and optimum phase position are extracted from incoming data
- Phase detection continuously running
- Jitter tracking limited by CDR bandwidth
  - With technology scaling we can make CDRs with higher bandwidths and the jitter tracking advantages of source synchronous systems is diminished
- Possible CDR implementations
  - Stand-alone PLL
  - “Dual-loop” architecture with a PLL or DLL and phase interpolators (PI)
  - Phase-rotator PLL
A primary difference between CDRs and PLLs is that the incoming data signal is not periodic like the incoming reference clock of a PLL.

A CDR phase detector must operate properly with missing transition edges in the input data sequence.
CDR Phase Detectors

- CDR phase detectors compare the phase between the input data and the recovered clock sampling this data and provides information to adjust the sampling clocks’ phase

- Phase detectors can be linear or non-linear

- Linear phase detectors provide both **sign and magnitude** information regarding the sampling phase error
  - Hogge

- Non-linear phase detectors provide **only sign** information regarding the sampling phase error
  - Alexander or 2x-Oversampled or Bang-Bang
  - Oversampling (>2)
  - Baud-Rate
Hogge Phase Detector

- Linear phase detector
- With a data transition and assuming a full-rate clock
  - The late signal produces a signal whose pulse width is proportional to the phase difference between the incoming data and the sampling clock
  - A Tb/2 reference signal is produced with a Tb/2 delay
- The ideal lock point is in the middle of a bit period, i.e. a $\pi$ or Tb/2 phase shift between clock and the data transition
- If the clock is sampling early, the late signal will be shorter than Tb/2 and vice-versa

\[ \text{[Razavi]} \]
Hogge Phase Detector

For phase transfer 0 rad is w.r.t optimal Tb/2 ($\pi$) spacing between sampling clock and data

- $\phi_e = \phi_{in} - \phi_{clk} - \pi$

- TD is the transition density – no transitions, no information
  - A value of 0.5 can be assumed for random data

$L_{\text{Tb/2 ref}}$ (Late – Tb/2 ref)

"1" Average Output Amplitude

Tb/2 ref

"-1" Average Output Amplitude

$K_{PD} = \frac{1}{\pi} (TD)$
Hogge Phase Detector Nonidealities

- **Flip-Flop Clk-to-Q delay** widens Late pulse, but doesn’t impact Tb/2 reference pulse
- CDR will **lock with a phase shift** (early sample clock) to equalize Tb/2 reference and Late pulse widths

[Razavi]
Hogge Phase Detector Nonidealities

- CDR phase shift compensated with a dummy delay element
- Other issues:
  - Need extremely high-speed XOR gates
  - Phase skew between Tb/2 reference and Late signals induces a “triwave” disturbance (ripple) on the control voltage

[Razavi]
PLL-Based CDR with a Hogge PD

- XOR outputs can directly drive the charge pump
- Need a relatively high-speed charge pump
Hogge PD Triwave on Vctrl

- Under nominal lock conditions, the control voltage integrates up and down with each transition.
- Periodic disturbance produces data-dependent jitter (DDJ), as the triangular pulse exhibits a nonzero net area.
- Since the data transition activity is random, a low frequency noise source is created that is not attenuated by the PLL dynamics.
Modified Hogge PD

- Two additional latches and XOR gates are added
- The first flip-flop, latch, and 2 XORs are identical to the original Hogge
- The second 2 latches and XORs produce an inverted version of the original triwave, which can drive a second parallel charge pump to produce a nominally zero net area waveform
Alexander (2x-Oversampled) Phase Detector

- Most commonly used CDR phase detector
- Non-linear (Binary) “Bang-Bang” PD
  - Only provides sign information of phase error (not magnitude)
- Phase detector uses 2 data samples and one “edge” sample
- Data transition necessary
  \[ D_n \oplus D_{n+1} \]
  - If “edge” sample is same as second bit (or different from first), then the clock is sampling “late”
  \[ E_n \oplus D_n \]
  - If “edge” sample is same as first bit (or different from second), then the clock is sampling “early”
  \[ E_n \oplus D_{n+1} \]
Alexander Phase Detector Characteristic (No Noise)

- Phase detector only outputs phase error sign information in the form of a late OR early pulse whose width doesn’t vary
- Phase detector gain is ideally infinite at zero phase error
  - Finite gain will be present with noise, clock jitter, sampler metastability, ISI

[Diagram showing the relationship between phase error and output pulse width]

[Lee]
Alexander Phase Detector Characteristic (With Noise)

- Total transfer characteristic is the convolution of the ideal PD transfer characteristic and the noise PDF
- Noise linearizes the phase detector over a phase region corresponding to the peak-to-peak jitter

$$K_{PD} \approx \frac{2}{J_{pp}}(TD)$$

- TD is the transition density – no transitions, no information
  - A value of 0.5 can be assumed for random data
Oversampling Phase Detectors

- Multiple clock phases are used to sample incoming data bits
- PD can have multiple output levels
  - Can detect rate of phase change for frequency acquisition
Mueller-Muller Baud-Rate Phase Detector

- Baud-rate phase detector only requires one sample clock per symbol (bit)

- Mueller-Muller phase detector commonly used

- Attempting to equalize the amplitude of samples taken before and after a pulse

Locked Condition: $h(\tau_k - T_b) = h(\tau_k + T_b)$
Early Clock: $h(\tau_k - T_b) < h(\tau_k + T_b)$
Late Clock: $h(\tau_k - T_b) > h(\tau_k + T_b)$
Mueller-Muller Baud-Rate Phase Detector

Phase Error:
\[ \Delta T_n = D_n \times D_{n-1} \times (\text{ERR}_n - \text{ERR}_{n-1}) \]

Phase detector output truth table

<table>
<thead>
<tr>
<th>( d_j )</th>
<th>( d_{j-1} )</th>
<th>( e_j )</th>
<th>( e_{j-1} )</th>
<th>( \Phi_{err_j} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>LATE</td>
</tr>
<tr>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>LATE</td>
</tr>
<tr>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>EARLY</td>
</tr>
<tr>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>EARLY</td>
</tr>
</tbody>
</table>

All other cases: HOLD

[Spagna ISSCC 2010]
Analog PLL-based CDR

\[ \frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}} \]

\[ K_P = I_c \cdot R \quad K_i = \frac{I_c}{C} \quad \omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}} \quad \zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2} \]
Analog PLL-based CDR

- CDR “bandwidth” will vary with input phase variation amplitude with a non-linear phase detector
- Final performance verification should be done with a time-domain non-linear model
Digital PLL-based CDR

[Sonntag JSSC 2006]
Digital PLL-based CDR

Open-Loop Gain:

\[ L(z^{-1}) = \left( \frac{K_{PD}KVK_{DPC}}{1 - z^{-1}} \right) \left( pHug + \frac{frug}{1 - z^{-1}} \right) z^{-N_{EL}}. \]

\[ \Phi_{\text{samp}} / \Phi_{\text{in}} = (L(e^{-j\omega})) / (1 + L(e^{-j\omega})) \]

[Sonntag JSSC 2006]
Digital PLL-based CDR

[Sonntag JSSC 2006]
Single-Loop CDR Issues

- Phase detectors have limited frequency acquisition range
  - Results in long lock times or not locking at all
  - Can potentially lock to harmonics of correct clock frequency
- VCO frequency range variation with process, voltage, and temperature can exceed PLL lock range if only a phase detector is employed
Phase and Frequency Tracking Loops

- Frequency tracking loop operates during startup or loss of phase lock
  - Ideally should be mostly off in normal operation
- Frequency loop bandwidth typically much smaller than phase loop bandwidth to prevent loop interaction
Frequency Detector

- Uses double-edged triggered input flip-flops with the Data signal sampling 2 quadrature clocks
- The Q output is then samples the I output
- For fast clocks relative to the data, $X_A$ will go high first and the output flip-flop will give a high value
- For fast clocks relative to the data, $X_B$ will go high first and the output flip-flop will give a low value
With large frequency offsets, the frequency detector output is unreliable.

Capture range $\sim <15\%$ frequency offset.
Analog Dual-Loop CDR w/ Two VCOs

- Frequency synthesis loop with replica VCO provides a “coarse” control voltage to set phase tracking loop frequency
- Frequency loop can be a global PLL shared by multiple channels
- Issues
  - VCO matching
  - VCO pulling
  - Distributing voltage long distances
Analog Dual-Loop CDR w/ One VCO

- Frequency loop operates during startup or loss of phase lock
  - Ideally should be mostly off in normal operation
- Input reference clock simplifies frequency loop design
- Care must be taken when switching between loops to avoid disturbing VCO control voltage and lose frequency lock
Phase Interpolator (PI) Based CDR

- Frequency synthesis loop produces multiple clock phases used by the phase interpolators.
- Phase interpolator mixes between input phases to produce a fine sampling phase:
  - Ex: Quadrature 90° PI inputs with 5 bit resolution provides sampling phases spaced by $90°/(2^5-1)=2.9°$
- Digital phase tracking loop offers advantages in robustness, area, and flexibility to easily reprogram loop parameters.
Phase Interpolator (PI) Based CDR

- Frequency synthesis loop can be a global PLL

- Can be difficult to distribute multiple phases long distance
  - Need to preserve phase spacing
  - Clock distribution power increases with phase number
  - If CDR needs more than 4 phases consider local phase generation
DLL Local Phase Generation

- Only differential clock is distributed from global PLL
- Delay-Locked Loop (DLL) locally generates the multiple clock phases for the phase interpolators
  - DLL can be per-channel or shared by a small number (4)
- Same architecture can be used in a forwarded-clock system
  - Replace frequency synthesis PLL with forwarded-clock signals
Phase Rotator PLL

- Phase interpolators can be expensive in terms of power and area
- Phase rotator PLL places one interpolator in PLL feedback to adjust all VCO output phases simultaneously
- Now frequency synthesis and phase recovery loops are coupled
  - Need PLL bandwidth greater than phase loop
    - Useful in filtering VCO noise
CDR Jitter Properties

- Jitter Transfer
- Jitter Generation
- Jitter Tolerance
CDR Jitter Model

\[
\begin{align*}
\phi_{out} &= \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}} \\
\phi_{in} &= \frac{I_C}{R} \quad K_i = \frac{I_C}{C} \quad \omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}} \quad \zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2}
\end{align*}
\]
Jitter Transfer

- Jitter transfer is how much input jitter “transfers” to the output
  - If the PLL has any peaking in the phase transfer function, this jitter can actually be amplified

\[
\frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}
\]
Jitter Transfer Measurement

System input clock with sinusoidal phase modulation (jitter)

\[ JTF(f) = 20\log\left( \frac{Output\text{Jitter}(f)}{Input\text{Jitter}(f)} \right) \]

[TrV89] [RaO91]

[Walker]
Jitter Transfer Specification

This specification is intended to control jitter peaking in long repeater chains.
Jitter generation is how much jitter the CDR “generates”
  - Assumed to be dominated by VCO
  - Assumes jitter-free serial data input

VCO Phase Noise: \[ H_{n\text{VCO}}(s) = \frac{\phi_{\text{out}}}{\phi_{n\text{VCO}}} = \frac{s^2}{s^2 + \left(\frac{K_{\text{Loop}}}{N}\right)RCs + \frac{K_{\text{Loop}}}{N}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

For CDR, N should be 1
Jitter Generation

High-Pass Transfer Function

Jitter accumulates up to time $\propto \frac{1}{\text{PLL bandwidth}}$

- SONET specification:
  - rms output jitter $\leq 0.01$ UI

[McNeill]
Open-Loop VCO Jitter – Self-Referenced

- Measure distribution of clock threshold crossings
- Plot $\sigma$ as a function of delay $\Delta T$
Open-Loop VCO Jitter – Self-Referenced

\[ \sigma_{\Delta T(OL)}(\Delta T) \approx \kappa \sqrt{\Delta T} \]

- Jitter \( \sigma \) is proportional to \( \sqrt{\Delta T} \)
- \( \kappa \) is VCO time domain figure of merit

[McNeill]
PLL limits $\sigma_{\Delta T}$ for delays longer than loop bandwidth $\tau_L$

$$\tau_L = \frac{1}{2\pi f_L} \quad \sigma_{\Delta T} = \kappa \sqrt{\frac{1}{2\pi f_L}}$$

If we refer the jitter to the reference (or transmit) clock, $\sigma_x$, the correlation between the clocks reduces the jitter sigma

$$\sigma_x = \frac{\sigma_{\Delta T}}{\sqrt{2}} = \kappa \sqrt{\frac{1}{4\pi f_L}}$$
Ref Clk-Referenced vs Self-Referenced

- Depending on how you measure jitter generation, you will get a different number, with the self referenced sigma being $\sqrt{2}$ higher.
Jitter Tolerance

- How much sinusoidal jitter can the CDR “tolerate” and still achieve a given BER?

\[ \phi_e(s) = \left(1 - \frac{\phi_{out}(s)}{\phi_{in}(s)}\right)\phi_{n.in}(s) \leq \frac{\text{Timing Margin}}{2} \]

As jitter tolerance is often specified in units of peak-to-peak jitter amplitude (UI_{pp})

\[ JTOL(s) = 2\phi_{n.in}(s) = \frac{TM}{\left(1 - \frac{\phi_{out}(s)}{\phi_{in}(s)}\right)} \]
Jitter Tolerance Measurement

While jitter tolerance testing quantifies the tolerance to sinusoidal jitter, often “stressed eyes” are used that have additional random and deterministic jitter to emulate realistic operating conditions.

Random and sinusoidal jitter are added by modulating the BERT clock.

Deterministic jitter is added by passing the data through the channel.

For a given frequency, sinusoidal jitter amplitude is increased until the minimum acceptable BER ($10^{-12}$) is recorded.

[Diagram showing signal generator, delay control, noisy clock, signal, BERT, backplane, test chip, and error count with sinusoidal and random noise added.]
Jitter Tolerance Measurement

\[ JTOL(s) = \frac{TM}{1 - \frac{\phi_{out}(s)}{\phi_{in}(s)}} \]

Flat region is beyond CDR bandwidth

(within CDR bandwidth)
Next Time

- Broadband amplifiers
  - Transimpedance amplifiers
  - Limiting amplifiers