ECEN689: Special Topics in High-Speed Links Circuits and Systems
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Lecture 30: CDRs

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Announcements

• Project Preliminary Report #2 due Monday April 26 in class

• Exam 2 is April 30

• Posted Fwd Clock Bandpass Filtering Paper

• Will Post
  • CDR Papers
  • Example PLL models
Agenda

- CDR overview
- CDR Phase Detectors
- Analog & Digital CDRs
Embedded Clock I/O Circuits

- **TX PLL**
- **TX Clock Distribution**
- **CDR**
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
  - Global PLL requires RX clock distribution to individual channels
Embedded Clocking (CDR)

PLL-based CDR

- Clock frequency and optimum phase position are extracted from incoming data
- Phase detection continuously running
- Jitter tracking limited by CDR bandwidth
  - With technology scaling we can make CDRs with higher bandwidths and the jitter tracking advantages of source synchronous systems is diminished
- Possible CDR implementations
  - Stand-alone PLL
  - “Dual-loop” architecture with a PLL or DLL and phase interpolators (PI)
  - Phase-rotator PLL
CDR Phase Detectors

- CDR phase detectors compare the phase between the input data and the recovered clock sampling this data and provides information to adjust the sampling clocks’ phase
- Phase detectors can be linear or non-linear
- Linear phase detectors provide both **sign and magnitude** information regarding the sampling phase error
  - Hogge
- Non-linear phase detectors provide **only sign** information regarding the sampling phase error
  - Alexander or 2x-Oversampled or Bang-Bang
  - Oversampling (>2)
  - Baud-Rate
Hogge Phase Detector

- Linear phase detector
- For phase transfer 0rad is w.r.t optimal Tb/2 spacing between sampling clock and data
  - $\phi_e = \phi_{in} - \phi_{clk}$
- TD is the transition density – no transitions, no information
  - A value of 0.5 can be assumed for random data

$$K_{PD} = \frac{1}{\pi} (TD)$$

(Late - Early)

Output Pulse Width

- [Razavi]
- [Lee]
Hogge Phase Detector Nonidealities

- **Flip-Flop Clk-to-Q delay** widens Late pulse, but doesn’t impact Early pulse
- **CDR** will **lock with a phase shift** to equalize to Early and Late pulse widths

[Razavi]
Hogge Phase Detector Nonidealities

- CDR phase shift compensated with a dummy delay element
- Other issues:
  - Need extremely high-speed XOR gates
  - Phase skew between Early and Late signals induces a “triwave” disturbance (ripple) on the control voltage

[Razavi]
Alexander (2x-Oversampled) Phase Detector

- Most commonly used CDR phase detector
- Non-linear (Binary) “Bang-Bang” PD
  - Only provides sign information of phase error (not magnitude)
- Phase detector uses 2 data samples and one “edge” sample
- Data transition necessary
  \[ D_n \oplus D_{n+1} \]
  - If “edge” sample is same as second bit (or different from first), then the clock is sampling “late”
  \[ E_n \oplus D_n \]
  - If “edge” sample is same as first bit (or different from second), then the clock is sampling “early”
  \[ E_n \oplus D_{n+1} \]
Alexander Phase Detector Characteristic (No Noise)

- Phase detector only outputs phase error sign information in the form of a late OR early pulse whose width doesn’t vary
- Phase detector gain is ideally infinite at zero phase error
  - Finite gain will be present with noise, clock jitter, sampler metastability, ISI

[Image of phase detector characteristic curve]
Alexander Phase Detector Characteristic (With Noise)

• Total transfer characteristic is the convolution of the ideal PD transfer characteristic and the noise PDF

• Noise linearizes the phase detector over a phase region corresponding to the peak-to-peak jitter

\[ K_{PD} \approx \frac{2}{J_{PP}} (TD) \]

• TD is the transition density – no transitions, no information
  • A value of 0.5 can be assumed for random data
Oversampling Phase Detectors

- Multiple clock phases are used to sample incoming data bits
- PD can have multiple output levels
  - Can detect rate of phase change for frequency acquisition

[Sheikholeslami]
Mueller-Muller Baud-Rate Phase Detector

- Baud-rate phase detector only requires one sample clock per symbol (bit)

- Mueller-Muller phase detector commonly used

- Attempting to equalize the amplitude of samples taken before and after a pulse

\[
\begin{align*}
\text{Locked Condition: } & h(\tau_k - T_b) = h(\tau_k + T_b) \\
\text{Early Clock: } & h(\tau_k - T_b) < h(\tau_k + T_b) \\
\text{Late Clock: } & h(\tau_k - T_b) > h(\tau_k + T_b)
\end{align*}
\]
Mueller-Muller Baud-Rate Phase Detector

Phase Error:
$$\Delta T_n = D_n \times D_{n-1} \times (ERR_n - ERR_{n-1})$$

Phase detector output truth table:

<table>
<thead>
<tr>
<th>(d_j)</th>
<th>(d_{j-1})</th>
<th>(e_j)</th>
<th>(e_{j-1})</th>
<th>(\varphi_{err_j})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>LATE</td>
</tr>
<tr>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>LATE</td>
</tr>
<tr>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>EARLY</td>
</tr>
<tr>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>EARLY</td>
</tr>
</tbody>
</table>

All other cases

[Spagna ISSCC 2010]
Analog PLL-based CDR

Model of PD

Model of Loop Filter

Model of VCO

“Linearized” $K_{PD}$

$\phi_{out} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}$

$K_P = I_C \cdot R$

$K_i = \frac{I_C}{C}$

$\omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}}$

$\zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2}$

[Lee]
Analog PLL-based CDR

- CDR “bandwidth” will vary with input phase variation amplitude with a non-linear phase detector
- Final performance verification should be done with a time-domain non-linear model
Digital PLL-based CDR

Bank of $W$ (word width) phase detectors, each producing a 2 bit output.

[Sonntag JSSC 2006]
Digital PLL-based CDR

Open-Loop Gain:

\[ L(z^{-1}) = \left( \frac{K_{PD}K_VK_{DPC}}{1 - z^{-1}} \right) \left( \text{phug} + \frac{frug}{1 - z^{-1}} \right) z^{-N_{EL}}. \]

\[ \Phi_{\text{samp}} / \Phi_{\text{in}} = \left( L(e^{-j\omega}) \right) / \left( 1 + L(e^{-j\omega}) \right) \]

[Sonntag JSSC 2006]
Digital PLL-based CDR

[Sonntag J SSC 2006]
Next Time

• CDR circuits