April 2, 2024

ECEN 721: Optical Interconnects

Final Project

Instructor: Sam Palermo

Project teams can consist of 1-3 students.

Project Topics

Project #1 – 10Gb/s PAM2 1km Optical Link Design

This project investigates the design of a 10Gb/s PAM2 1km optical link for a target BER=10^{-12}. A complete link budget should be constructed considering the chosen optical source, channel losses, optical channel, and receiver sensitivity. The optical source can either be a directly modulated VCSEL or an externally modulated CW laser with either a MZM, EAM, or ring resonator modulator (carrier-injection or carrier depletion). The photodetector can either be p-i-n (waveguide or discrete), APD, or OA/p-i-n. However, preference is given to a p-i-n detector. Key specs for the receiver decision element are: $1mV_{rms}$ noise, 1mV offset, and 20fF total input capacitance. The driver and receiver front-end circuits should be designed at the transistor level. Note, you don't have to design the decision element. 10Gb/s eye diagrams should be produced with equivalent circuit models for the optical source and photodetectors. Show eye diagrams at both the transmitter output and the final receiver output. A key metric of the link design is the overall power efficiency (mW/Gbps). Note, for an externally-modulated system this should include the CW laser power.

Project #2 – 112GS/s Time-Domain ADC

This project involves the design of a high-speed time-domain ADC that is enabled through voltage-to-time converter (VTC) and time-to-digital converter (TDC) circuits. This time-interleaved ADC should operate at 112GS/s with 7b resolution and achieve sub-40fJ/conv.-step FOM. The ADC input interleaver network should achieve a minimum 56GHz bandwidth. The impact of metastability should be studied in the context of a 224Gb/s ADC-based PAM4 transceiver operating over a channel with at least 40dB loss at Nyquist.

Project #3 – Low-Jitter Wideband 5-10GHz PLL

This project involves the design of a low-jitter wideband PLL. The main specs are:
Output Frequency Range = 5 - 10GHz (All frequencies)
Fixed N=16 loop division factor with a scalable reference clock (312.5 – 625MHz)
Loop Bandwidth between 4 - 5MHz
Output Jitter < $100fs_{rms}$ integrated over a 10kHz – 10MHz bandwidth

Project #4 – 224Gb/s Coherent Transmitter Driver

This project involves the design of a driver for a 224Gb/s dual-polarization QAM16 coherent transmitter. The 28GBaud transmitter should support PAM-4 modulation at a minimum $2V_{ppd}$ output swing, allowing for 224Gb/s operation with a silicon photonic dual-polarization coherent modulator. A complete link model should be constructed with models for the receiver-side coherent demodulator and high-bandwidth TIA receiver and operation with BER<10-4 should be verified.

Project #5 – Topic of Your Choice

I welcome any project suggestions related to optical interconnects circuits and systems.

Important Dates

- April 16 Preliminary Report. This will be HW4.
- Apr 30 Final Report Due
- May 7 Project Presentation Due

Preliminary Report Required Sections

1. Motivation and Project Overview
2. Literature Survey
3. Proposed Architecture
    a. This can change for the final report
4. Initial Simulation Results
5. Plan of Work
    a. A description of what will be completed for the final report

Final Report Required Sections

1. Motivation and Project Overview
2. Literature Survey
3. Architecture
4. Simulation Results
    a. This section must include a Table comparing your design with current references
5. Conclusion

The Project Presentation should include the same sections as the final report.