ECEN721: Optical Interconnects Circuits and Systems
Spring 2024

Lecture 14: Analog MZM Driver with Linearization

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Announcements

- Exam 2 is on Apr. 23
  - In class
  - One double-sided 8.5x11 notes page allowed
  - Bring your calculator
  - Covers through Lecture 12

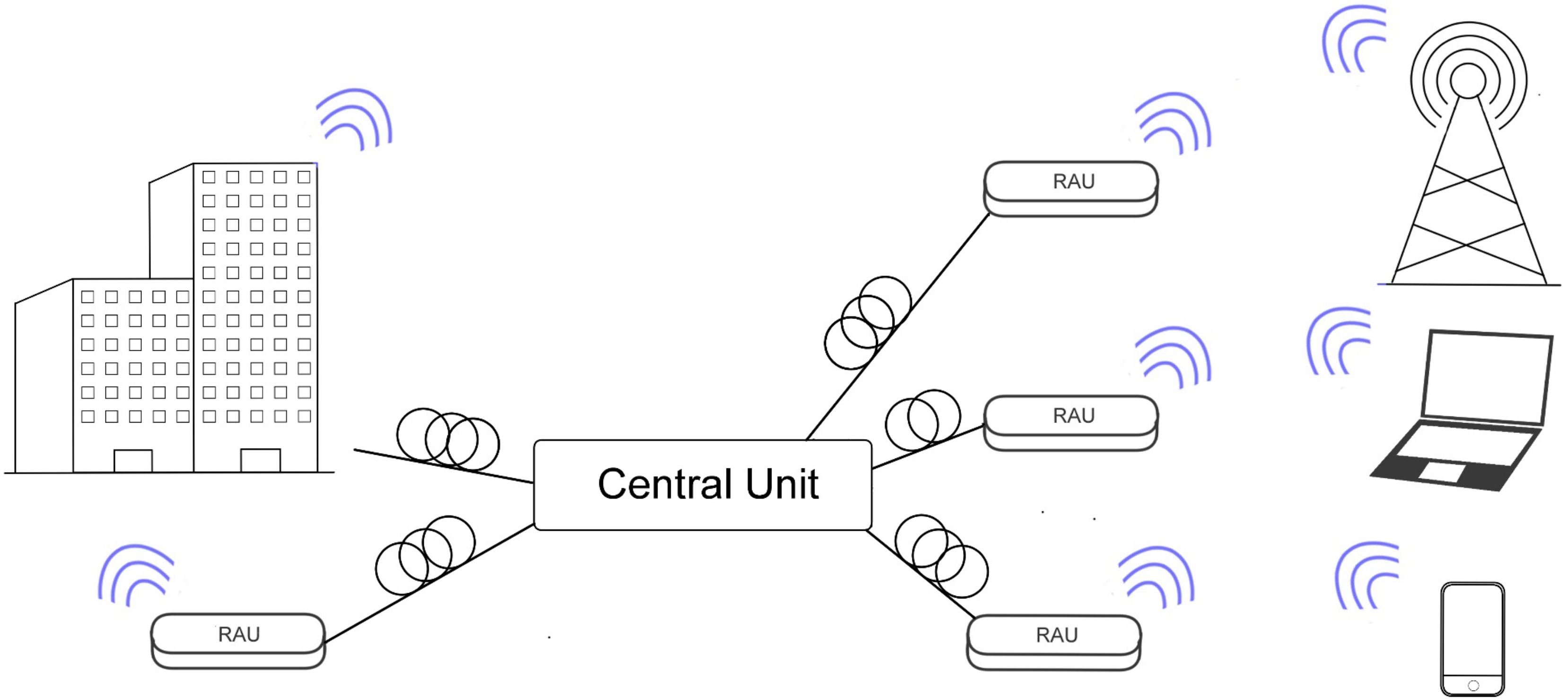
- Project Report Due Apr 30

- Project Presentations May 7 (3:30PM-5:30PM)

Outline

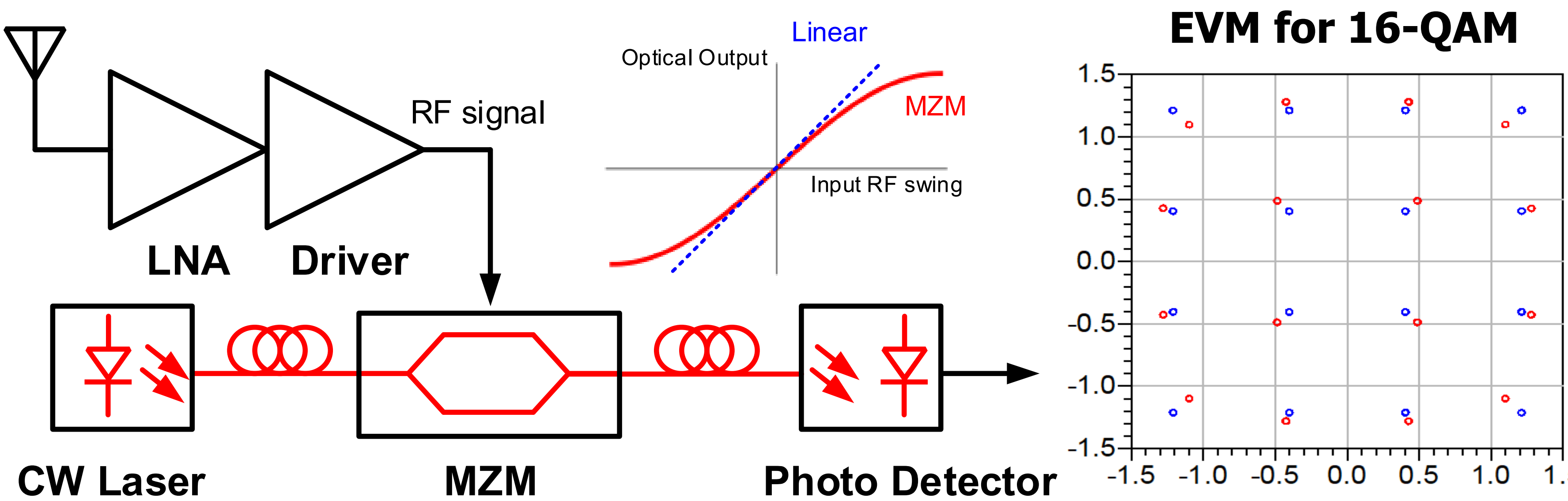
- Motivation
- Driver Design
- Measurement Results
- Conclusion

Radio-Over-Fiber Systems



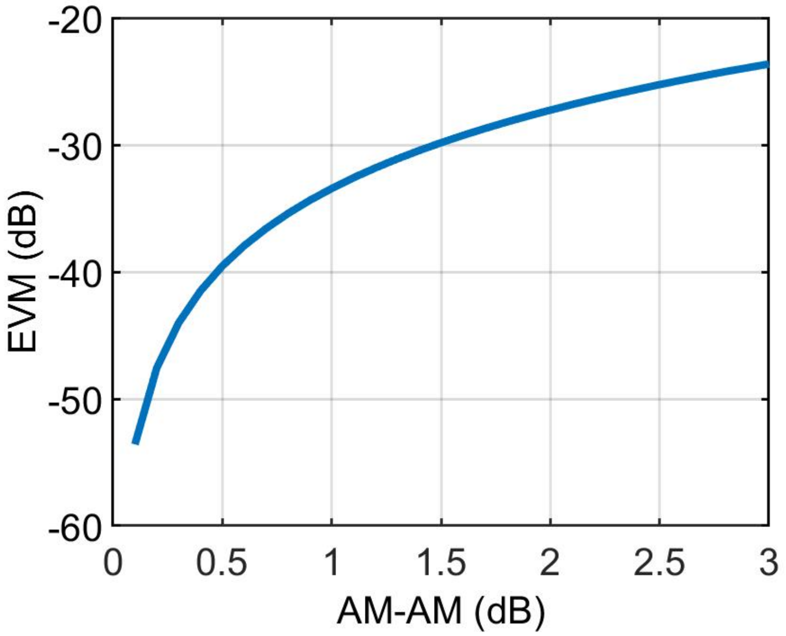
- Remote antenna units
- Indoor wireless communications
- 5G cellular communications

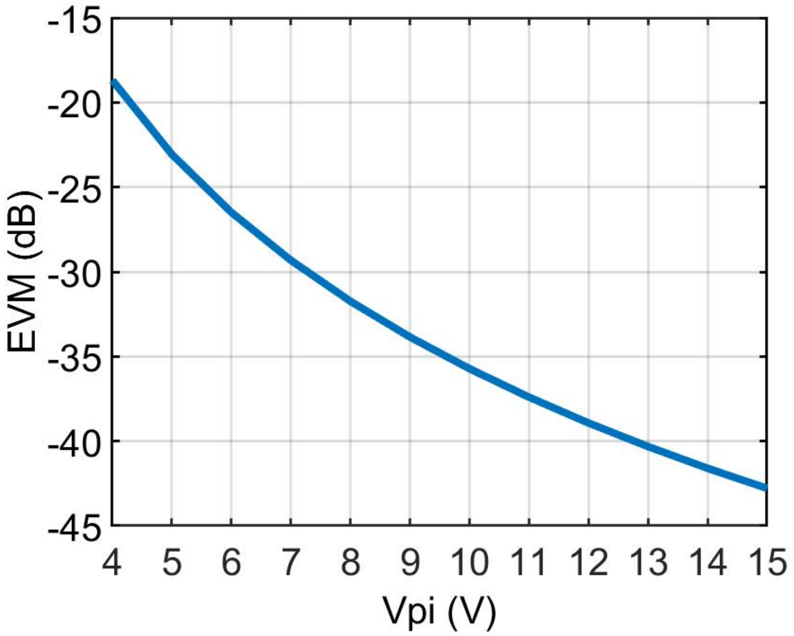
Nonlinearity in RoF Systems



- MZM cosine transfer function
  - Major source of nonlinearity
  - AM-AM compression

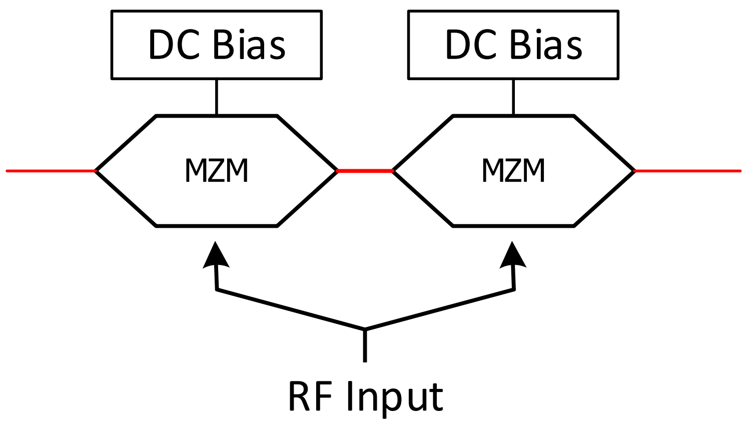
16-QAM EVM vs AM-AM

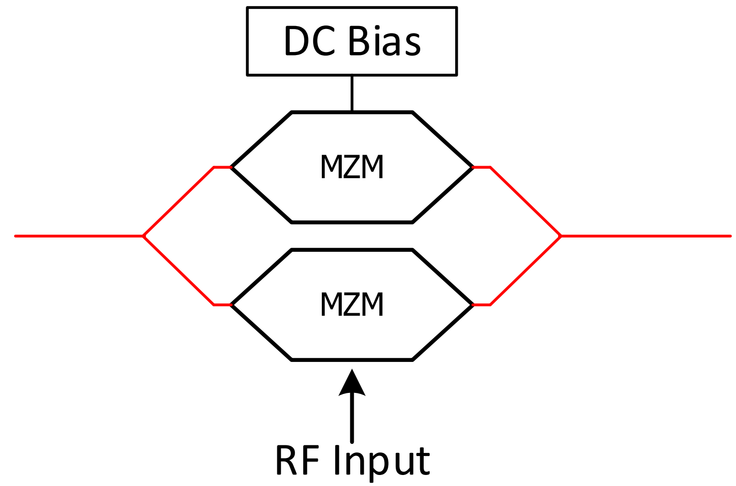




- Assuming ideal cosine model for MZM
- EVM degrades when AM-AM compression increases
- Lower V_π MZM has higher gain, but more nonlinearity

MZM Linearization Approaches





- Optical domain linearization occupies large PIC area
- Electrical domain linearization approaches
  - Arcsine function from square law of transistor
  - Polynomial predistortion
  - IM3 injection
  - Diode-based predistortion
- Proposed programmable linearizer is able to compensate AM-AM and is highly tunable to generate predistortion

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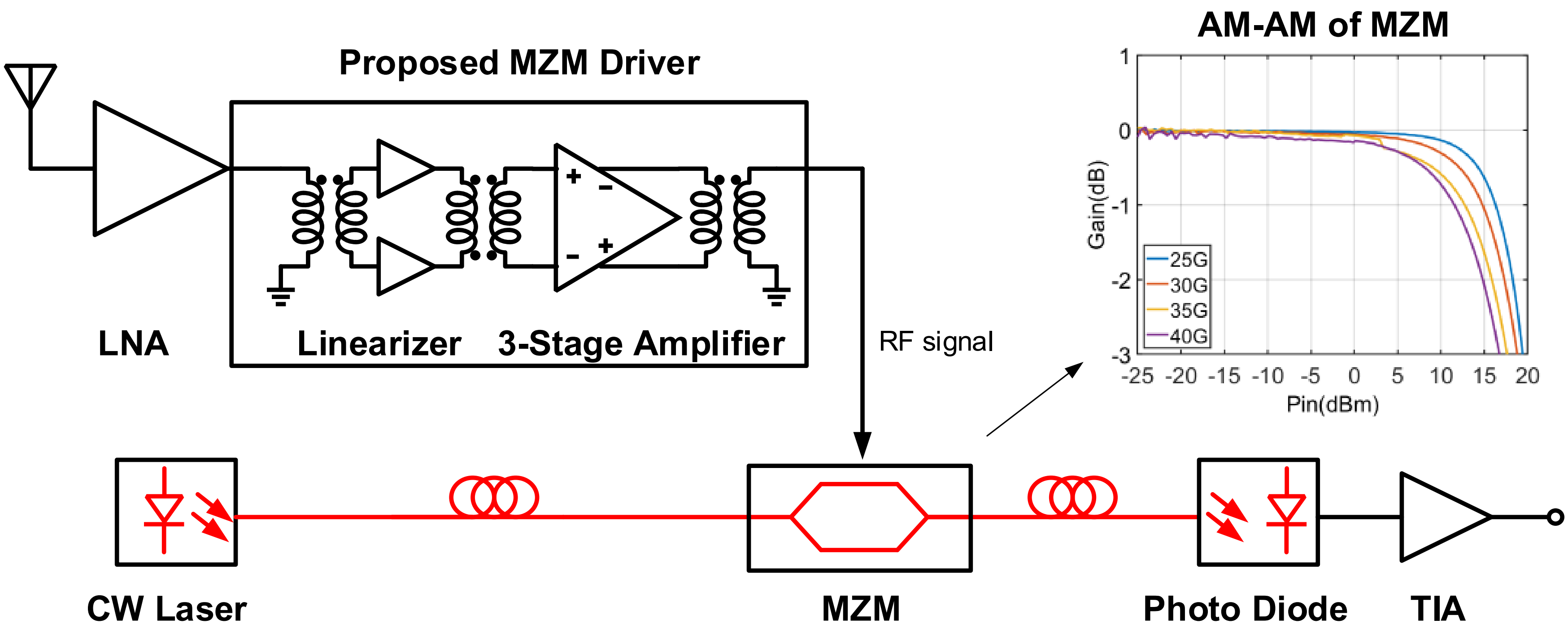
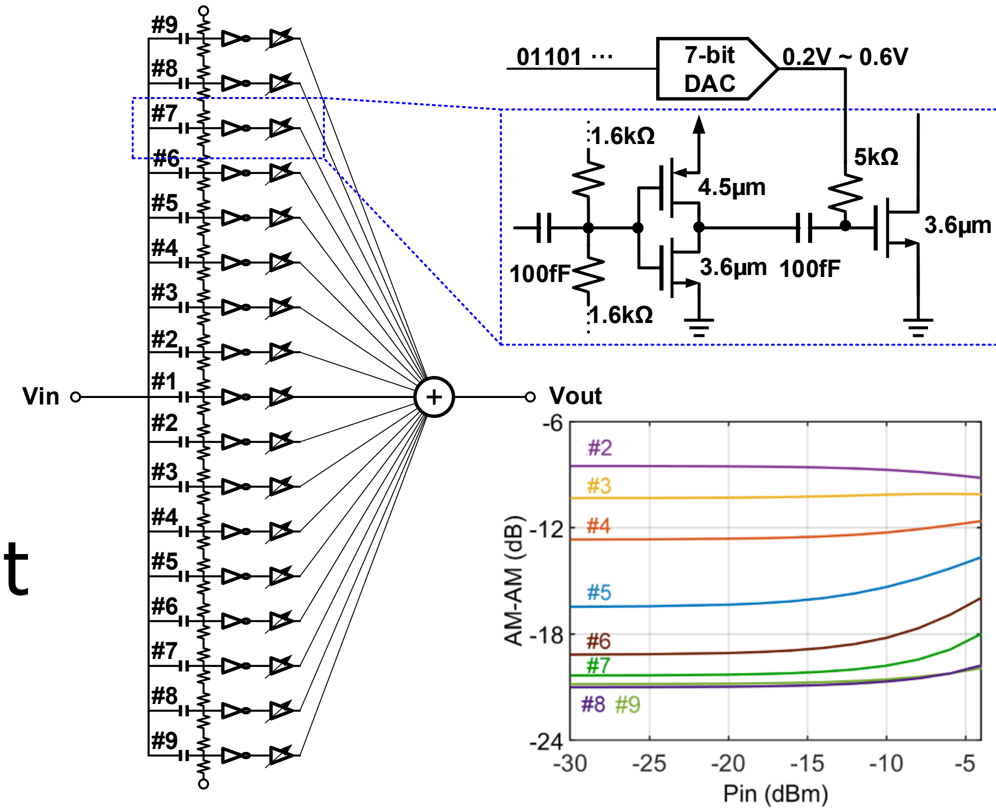
MZM Driver Architecture



- Programmable inverter-based amplifier linearizer generates predistortion to compensate MZM nonlinearity
- 3-stage amplifier provides gain to deliver 12dBm linear output power to drive MZM

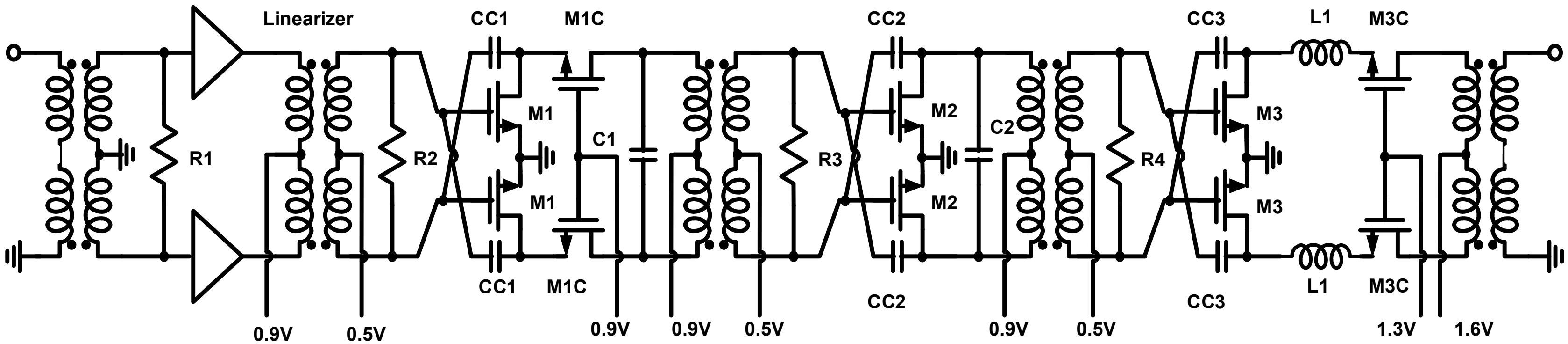
Inverter-Based Amplifier Linearizer

- 17 unit segments consisting of inverter-based amplifiers
- Segments 1-3 provide gain without major expansion



- Segments 4-9 provide signal expansion at progressively larger input power levels

CMOS Driver



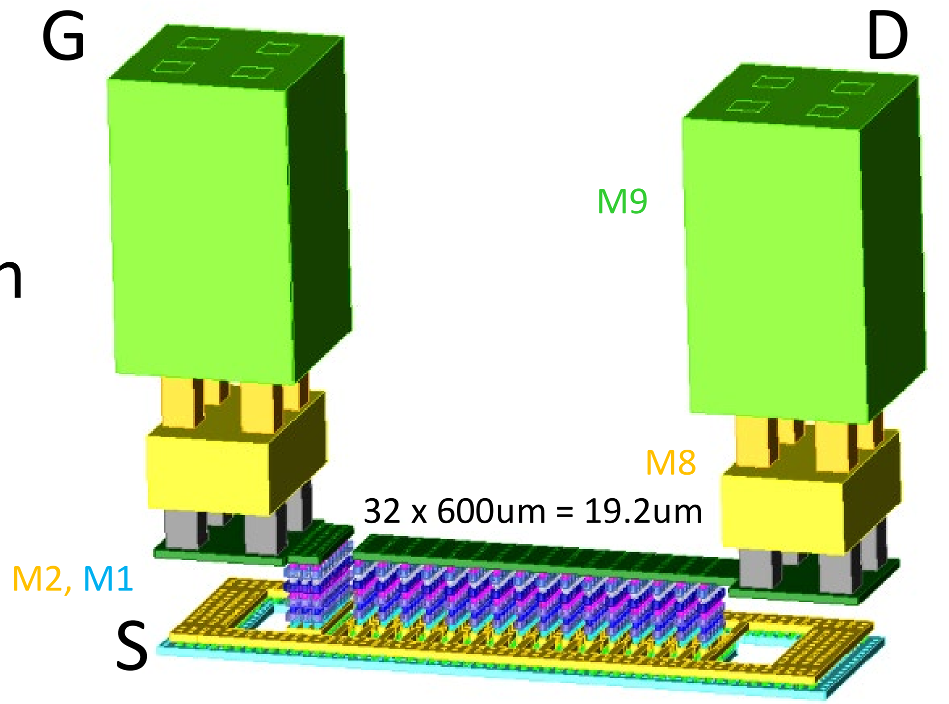
R1	R2	CC1	M1	M1C	C1	R3
160Ω	160Ω	30fF	19.2µm x 5	19.2µm x 5	60fF	50Ω

CC2	M2	C2	R4	CC3	L1	M3	M3C
20fF	19.2µm x 10	50fF	50Ω	40fF	60pH	19.2µm x 24	19.2µm x 18

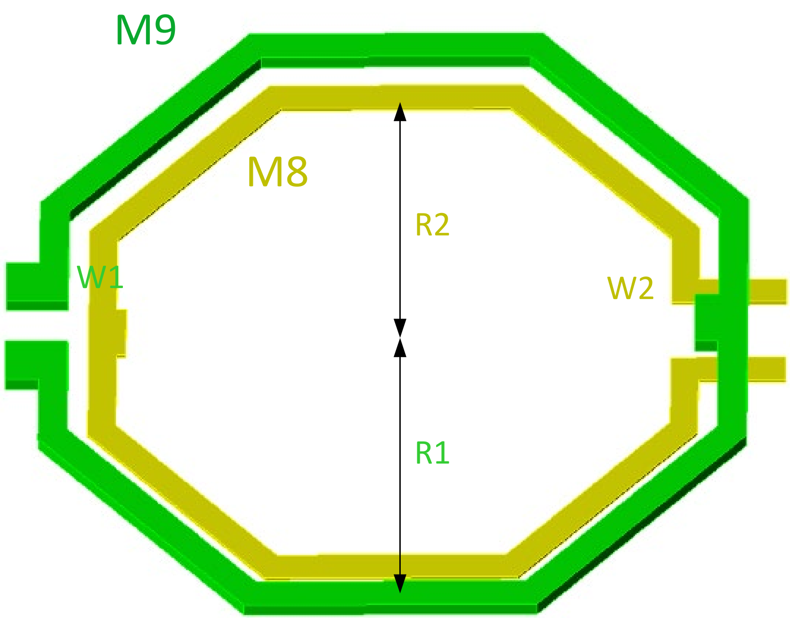
- 3 pseudo-differential common-source amplifier stages
- Capacitive neutralization improves reverse isolation
- Cascode structures in first stage improves stability and in last stage allows for operation with a higher supply
- Inter-stage and output-stage matching implemented with symmetrical magnetically coupled resonator technique

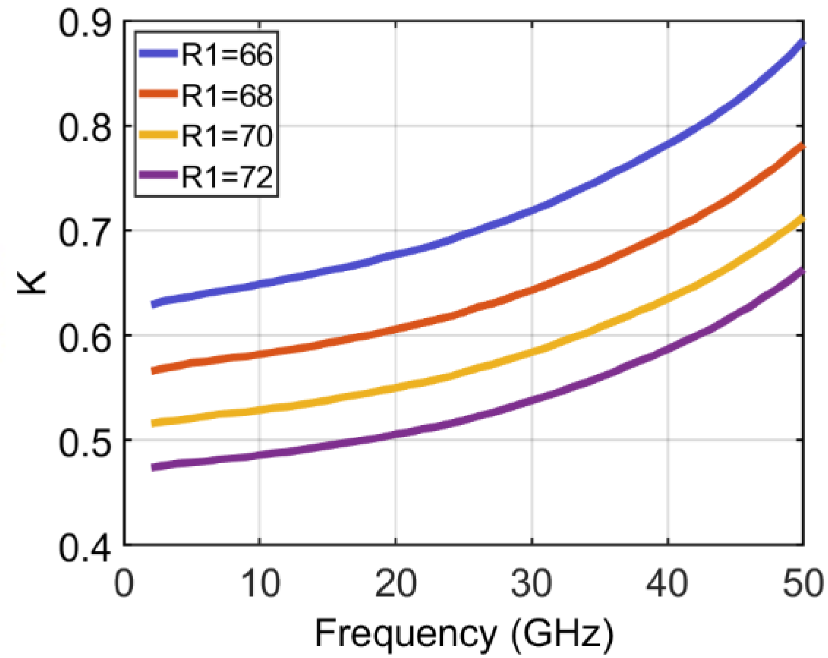
28nm CMOS Unit Cell Layout

- Unit cell methodology allows for easy scaling of each amplifier stage
  - 32 600nm width fingers
  - Parasitics minimized with higher metal routing for drain connection
  - Gate resistance reduced with double-sided connection
  - Source impedance reduced with stacked M1/2 layers



Mutual coupling resonator (MCR)

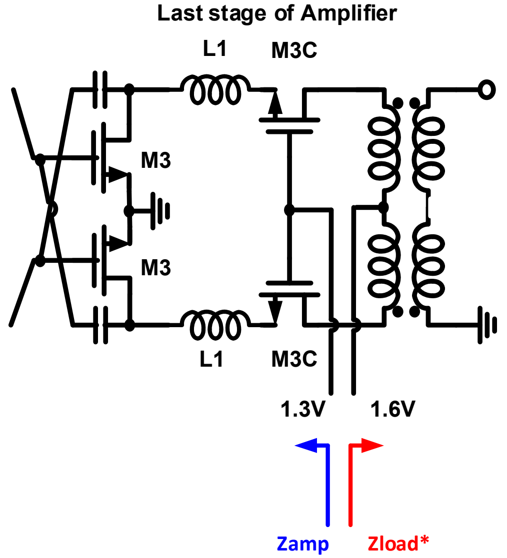


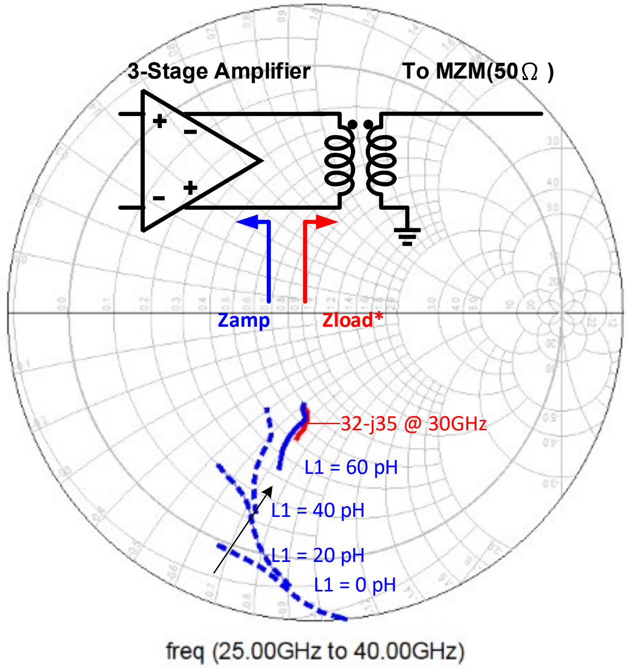


- Adjusting Coupling factor by tuning radius
- Requirement for zero gain ripple

$$k'^2\left(Q^2+1\right)=1$$

Output matching





- Inductor L1 adopted to tune the impedance Zamp
- Conjugate matching for power delivery and output return loss

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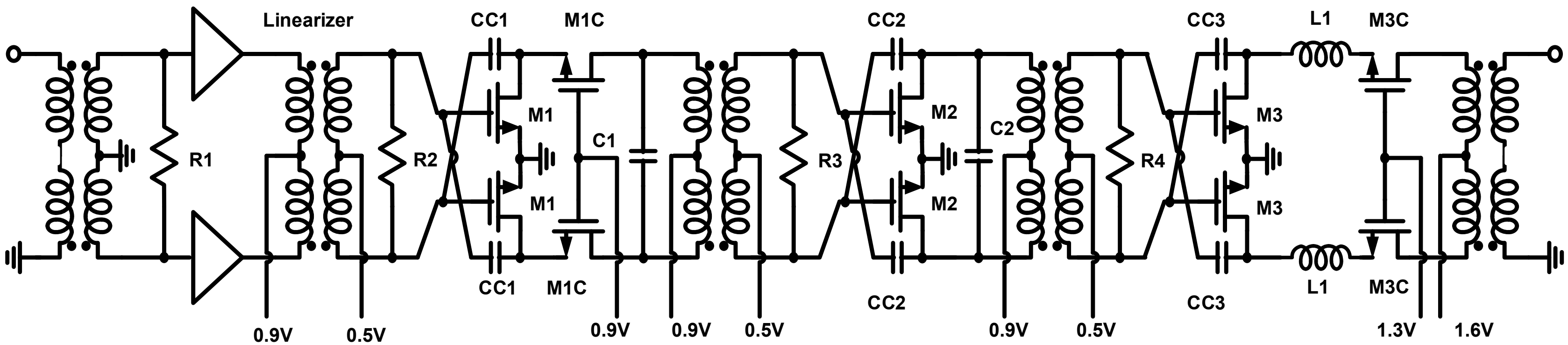
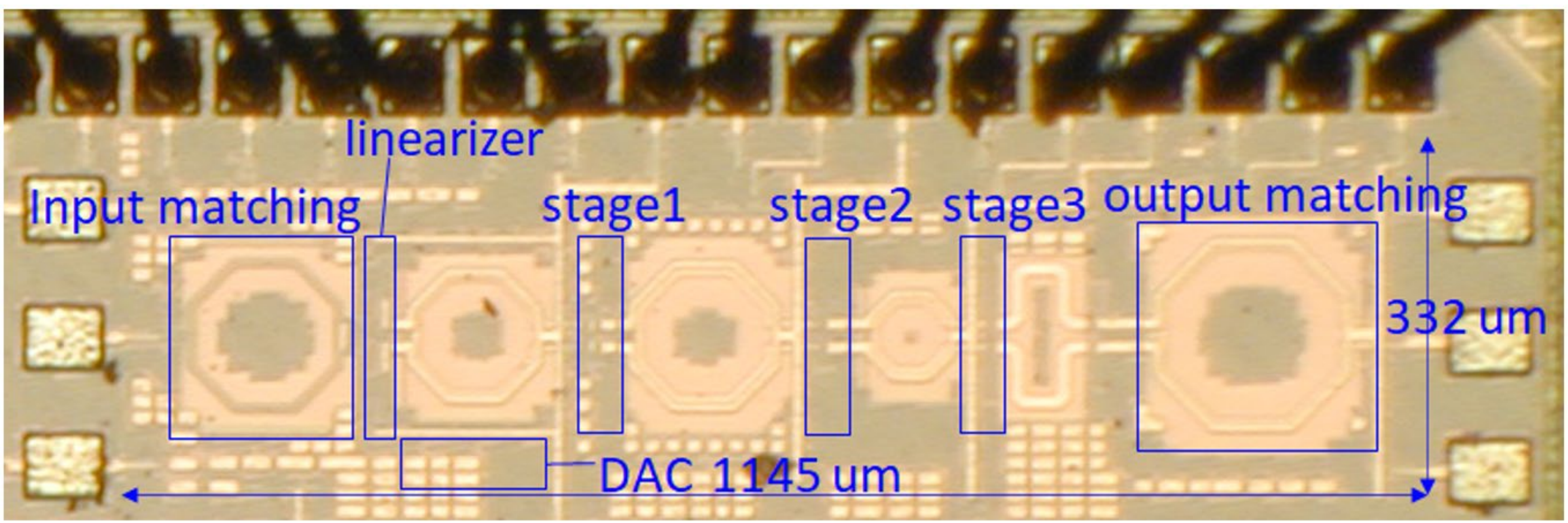
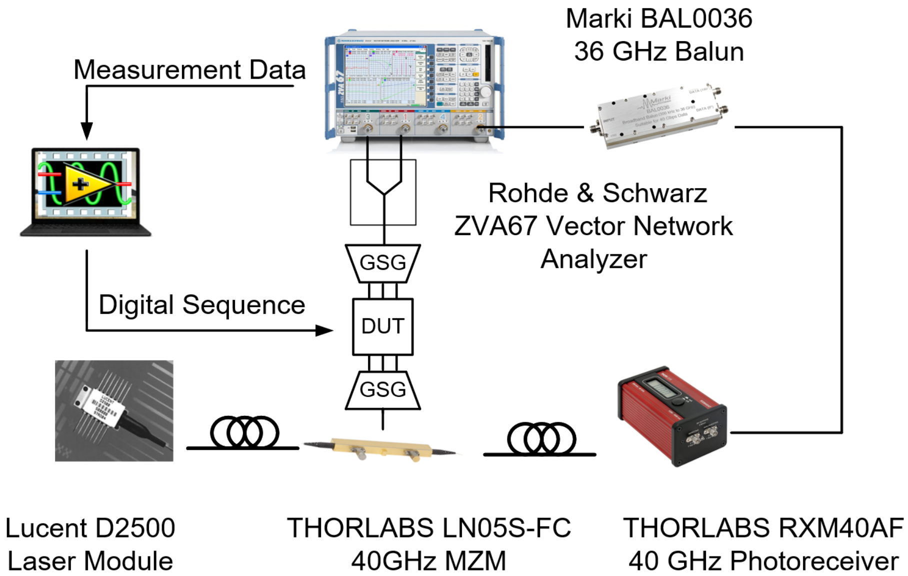
28nm CMOS Prototype

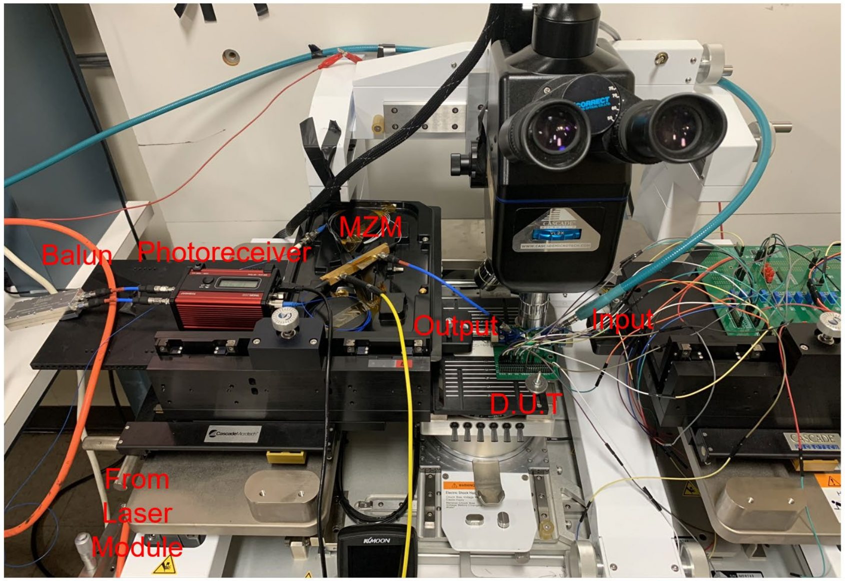




- GSG probe pads for high-speed input and output
- DC supplies and serial control signals applied via wirebonds to PCB

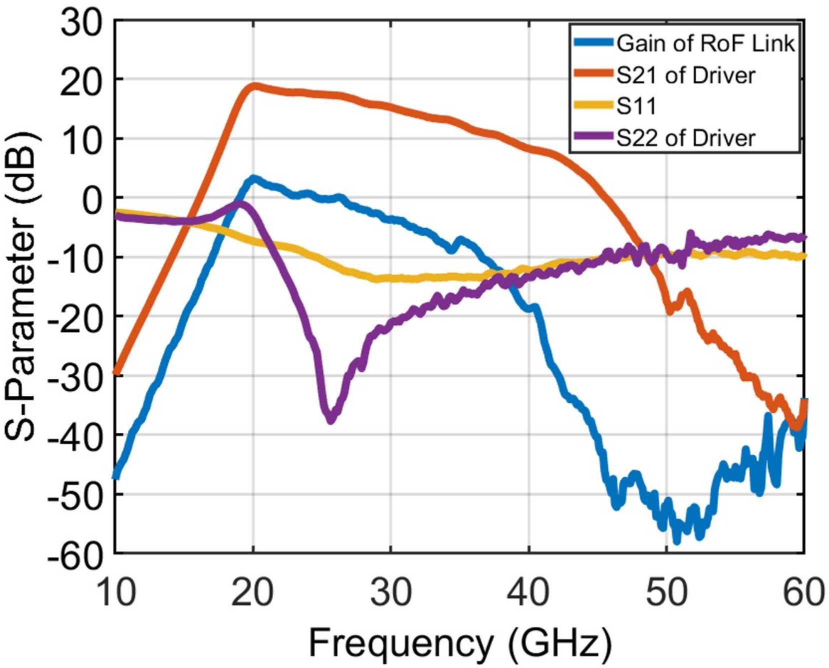
Test Setup

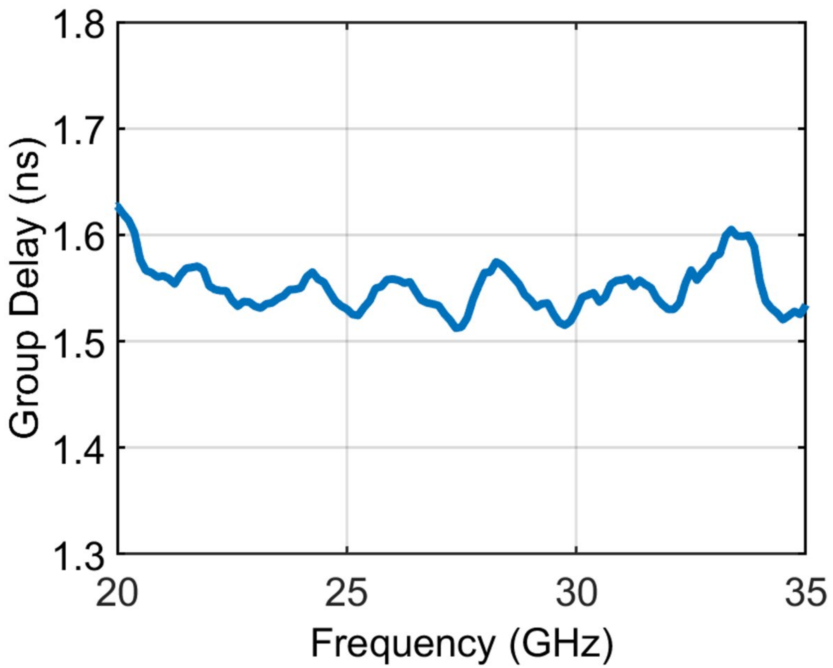




- 40GHz LiNbO3-MZM with 7V RF V_{π} at 30GHz
- MZM biased at quadrature point

S-Parameters & Group Delay

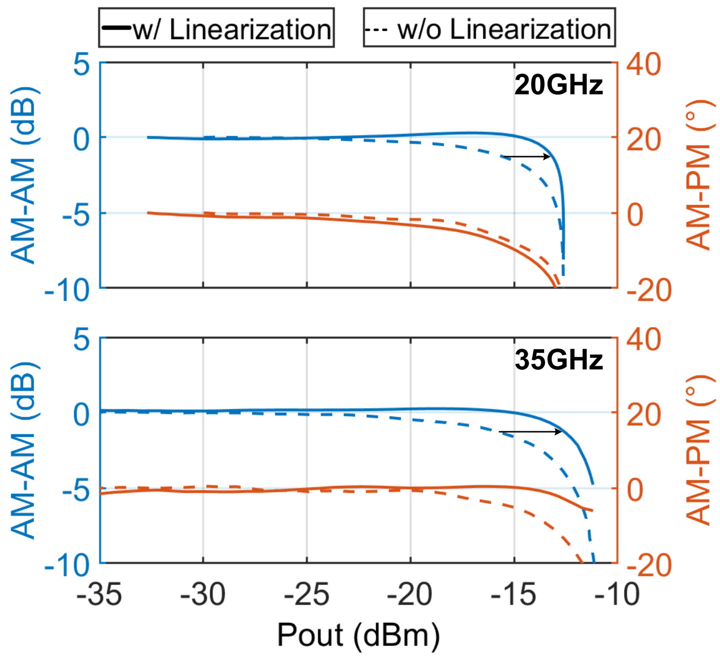




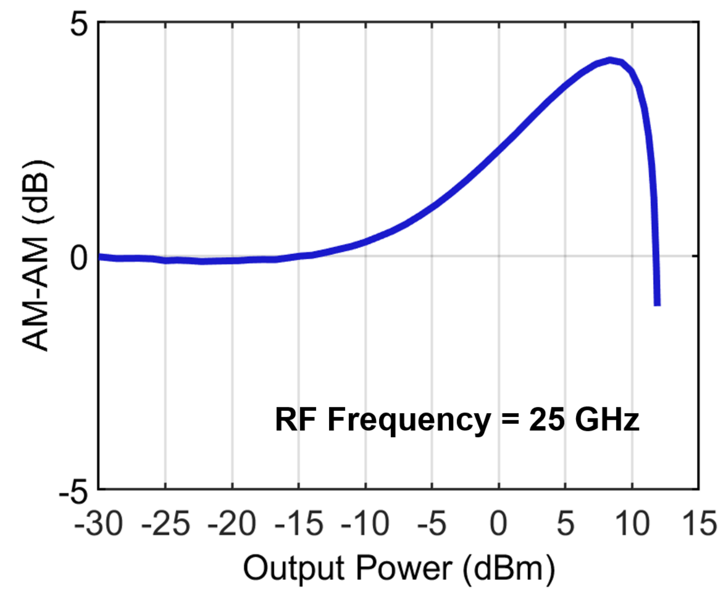
- 20-35GHz 3dB bandwidth with max 18dB gain
- Group delay variation of the entire RoF link is <115ps within the 20-35 GHz bandwidth

AM-AM Compensation

RoF Link AM-AM & AM-PM

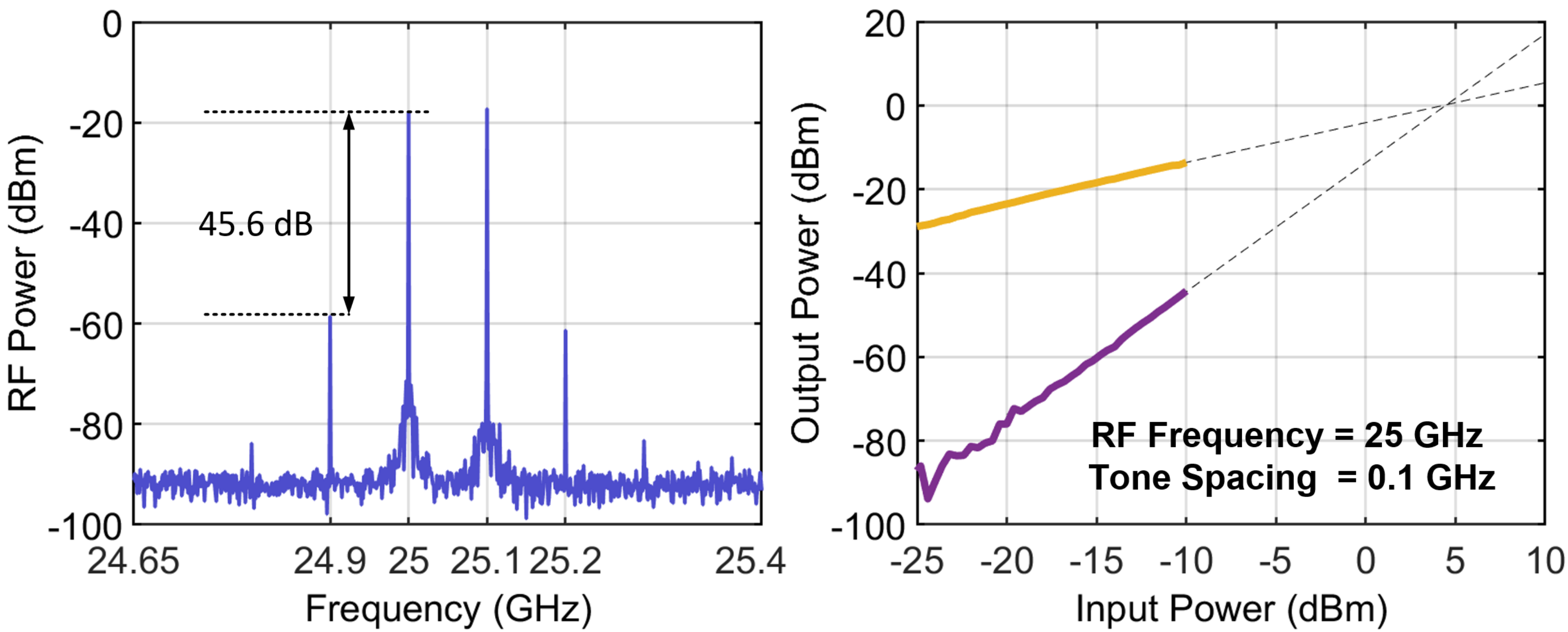


MZM Driver AM-AM w/ Linearizer



- Activating linearizer allows for 3dB OP1dB extension
- Driver delivers 12dBm output power with expansive response that compensates MZM compression

Two-Tone Measurements



- 4.1dBm IIP3 for entire RoF link

Summary Table

References	[Hosseinzadeh RFIC 2019]	[Sadhwani JLT 2003]	[Okyere Texas Symposium on 2017]	This Work
Technology	Si-SiGe	CMOS 180nm	65nm CMOS	28nm CMOS
Frequency	0.5-20GHz	0.28GHz	1GHz	20-35GHz
Power Consumption	1700mW*	162mW	49.2mW	180mW
Max Voltage Swing	$2V_{pp}$	N/A	N/A	$2.5V_{pp}$
IIP3	22dBm	6.8dBm	N/A	4.1dBm
Supply Voltage	2.5/3.3V	1.8V	N/A	0.9/1.6V
Power Efficiency**	11.76 GHz/W	1.73GHz/W	N/A	194.44GHz/W
Technique	IM3 Injection	Adaptive Predistoriton	Polynomial Predistortion	Predistortion

*Total power of 4 stages

**Power Efficiency = Max Frequency / Power Consumption

Conclusion

- A power-efficient 28nm CMOS MZM driver for an external MZM is implemented
- 20-35GHz bandwidth and 2.5V_{pp} output swing is achieved
- Programmable linearizer is able to extend OP1dB by 3dB and has the flexibility to support different MZM types